Small signal combination IC for colour TV

TDA8304

FEATURES

- Gain controlled vision IF amplifier
- Synchronous demodulator for negative and positive demodulation
- AGC detector operating on peak sync amplitude for negative demodulation and on vision peak white level for positive demodulation
- Tuner AGC
- AFC circuit with on/off-switch
- Video preamplifier
- Video switch to select either the internal video signal or an external video signal
- Horizontal oscillator and synchronization circuit with two control loops
- Vertical synchronization (divider system), ramp generator and driver with automatic amplitude adjustment for 50 and 60 Hz
- Transmitter identification (mute)
- Sandcastle pulse generation
- Auto VCR switch
- 50/60 Hz identification

GENERAL DESCRIPTION

The TDA8304 possesses the capability to demodulate IF signals having either positive or negative-going video information. It is housed within a 32-pin encapsulation. The device includes a three-stage video IF amplifier, AFC and AGC circuitry, integral three-level sandcastle pulse generator, fully synchronized horizontal and vertical time bases with drive circuits, a video switch and a transmitter identification/mute circuit. A functional colour TV receiver can thus be realised with the addition of a tuner, audio demodulator and amplifier, chrominance decoder and respective line and field deflection circuitry.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA8304	32	DIL	plastic	SOT201

FUNCTIONAL DESCRIPTION

Video IF amplifier, demodulator and video amplifier

Each of the three AC-coupled IF stages permits the omission of DC feedback and possesses a control range in excess of 20 dB.

The IF amplifier is followed by a passive synchronous demodulator providing a regenerated carrier signal. This is limited by a logarithmic limiter circuit prior to its application to the demodulator. Improved picture synchronization is provided by a wider bandwidth together with improved video amplifier linearity. The video amplifier contains also a white spot inverter and a noise clamp which limits interference pulses to a point below the peak sync level.

AFC-circuit

The reference signal for the AFC quadrature demodulator can also be acquired from the tuned circuit of the IF synchronous demodulator because an accurate 90° phase shift is realised internally. In this way only one tuned circuit needs to be applied and only one adjustment has to be carried out. The AFC output is affected by the asymmetrical frequency spectrum of the signal fed to the quadrature demodulator, which is determined by the SAW filter characteristic. To overcome this video frequency dependency of the AFC output, the demodulator output is followed by a sample-and-hold circuit.
For the reception of negative-going signals, the output is sampled only during peak sync (where a non-modulated carrier is present). When receiving signals with positive modulation the AFC is continuously active but extensively filtered. Substantial noise will be present on the quadrature demodulator input signal during reception of very weak signals. This noise has an asymmetrical frequency spectrum (with respect to the IF carrier) causing an offset in the AFC output voltage. This effect can be minimized by applying a notch in the demodulator tuned circuit. The sample-and-hold circuit is followed by an amplifier with high output impedance. The steepness of the of the AFC control voltage can be lowered by applying load resistors from the output to the supply and to ground. The AFC output is switched off when the AFC sample pin (22) is connected to ground.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_P	supply voltage (pin 8)		10	12	13.2	V
I_P	supply current (pin 8)		90	115	140	mA
I_{start}	start current (pin 12)	note 1	-	6.5	9	mA
Video						
$V_{9\text{-}10(rms)}$	IF sensitivity (RMS value)	note 2	25	40	65	µV
$G_{9\text{-}10}$	IF gain control range		-	74	-	dB
S/N	signal-to-noise ratio	input signal = 10 mV	52	58	-	dB
V_{21}	AFC output voltage swing		10.5	-	11.5	V
Video switch						
$V_{16(p\text{-}p)}$	internal video input (peak-to-peak value)	V_O = 2.5 V(p-p)	-	2	-	V
$V_{13(p\text{-}p)}$	external video input (peak-to-peak value)	V_O = 2.5 V(p-p)	-	1	-	V
$V_{15(p\text{-}p)}$	video output signal (peak-to-peak value)		2.3	2.5	2.7	V
Sync						
V_{28}	required sync pulse amplitude	note 3	200	750	-	mV
I_{30}	required input current during flyback pulse		0.1	-	2	mA
V_{30}	sandcastle output during burstkey horizontal blanking vertical blanking		 8 4 2.1	 - 4.4 2.5	 - 5 2.9	 V V V
V_{25}	video transmitter identification output no signal condition signal condition		 - -	 0.3 9.8	 - -	 V V
V_5	vertical feedback for DC voltage		2.9	3.3	3.7	V
$V_{5(p\text{-}p)}$	vertical feedback for AC voltage (peak-to-peak value)		-	1	-	V

Notes to the quick reference data

1. Supplying a current of 9 mA to pin 12 starts the horizontal oscillator. This current can be obtained via a bleed circuit from the mains rectifier whilst the main supply for the device (V_{cc}) is obtained from the horizontal output stage. The load current of the driver must be added to the value given.
2. On set AGC.
3. The minimum value is obtained by connecting a 1.8 kΩ resistor between pins 15 and 28. The slicing level can be varied by changing the value of this resistor (higher resistor value results in larger value of the minimum sync pulse amplitude). The slicing level is independent of the video information.

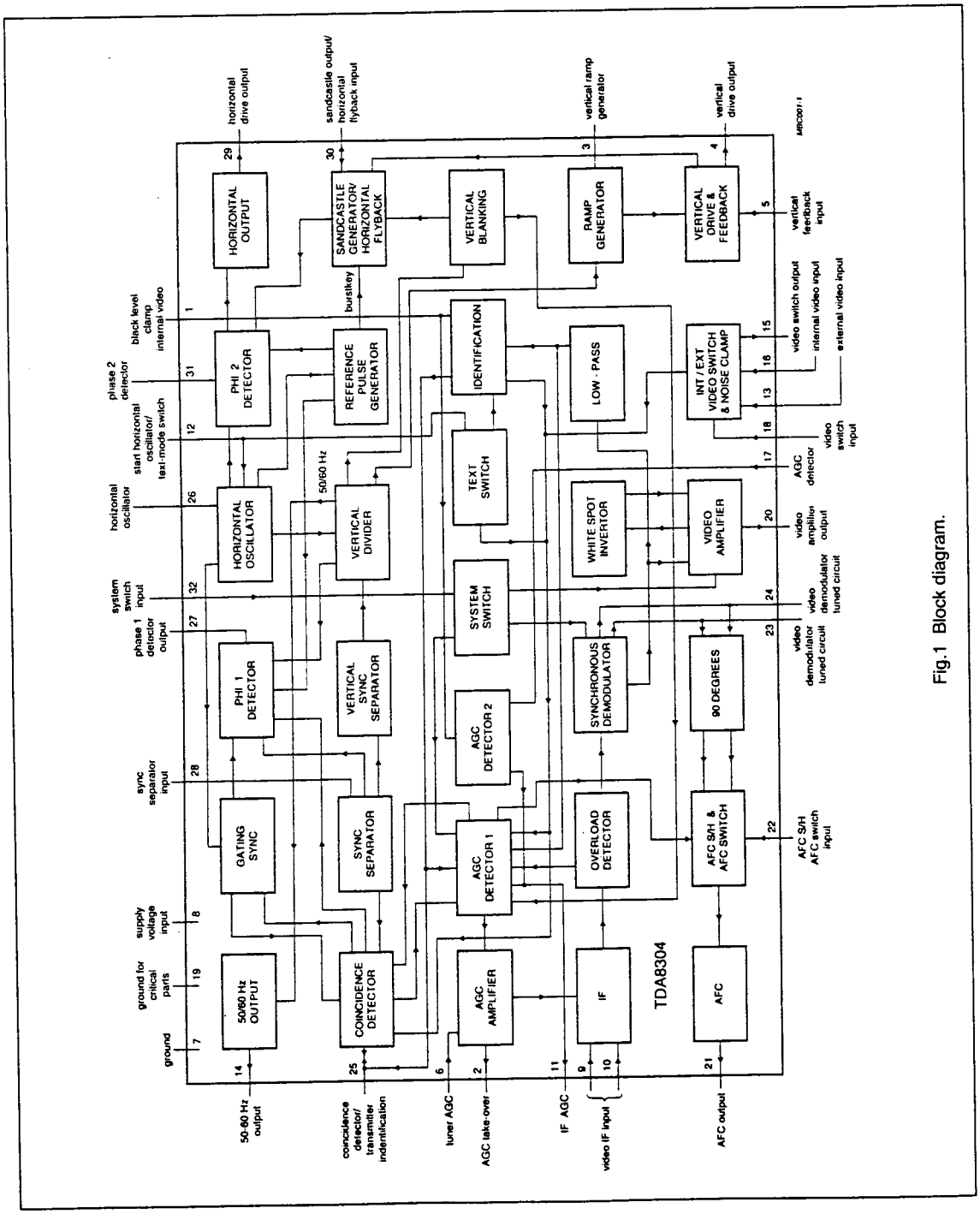


Fig.1 Block diagram.

PINNING

PIN	DESCRIPTION
1	black level clamp internal video
2	tuner take-over
3	vertical ramp generator
4	vertical drive
5	vertical feedback
6	tuner AGC
7	ground
8	supply voltage input
9	video IF input
10	video IF input
11	IF AGC
12	start horizontal oscillator/text-mode switch
13	external video input
14	50 - 60 Hz output
15	video switch output
16	internal video input
17	AGC detector
18	video switch input
19	ground for some critical parts
20	video amplifier output
21	AFC output
22	AFC S/H, AFC switch input
23	video demodulator tuned circuit
24	video demodulator tuned circuit
25	coincidence detector/transmitter identification
26	horizontal oscillator
27	phase 1 detector
28	sync separator input
29	horizontal drive output
30	sandcastle output/horizontal flyback input
31	phase 2 detector
32	system switch input

AGC circuit

For signals employing negative modulation the AGC detector operates on peak sync level and on peak white level with those having positive modulation. Selection is facilitated by the system switch (pin 32), see Table 1.

The charge current at positive modulation (see Table 2) is only present during the vertical sync or when the level at pin 1 drops 200 mV below the level of pin 17 as a result of input signal variations. To obtain rapid AGC action when executing a search tuning operation when the circuit is set for peak white AGC, the charge current is increased to 55 µA until the detection of a transmitted signal. With an AGC capacitor of 6.8 µF the video tilt will be < 2% for positive and for negative modulated signals.

VCR switch

The TDA8304 has an auto VCR-switch facility. Due to the inherent instability of signals from a VCR, the horizontal time constant should be shorter to prevent loss of horizontal synchronization in the early part of the scan. Provision is therefore incorporated (in the internal video mode) to automatically switch the short time constant such that a strong signal instigates the 'VCR' mode and a weak signal triggers the 'TV' mode. The phase detector is gated during the 'TV mode' and operates with a long time constant. The phase detector is not gated in the 'VCR' mode and operates with a short time constant. The TDA8304 is active in the 'VCR' mode only at reception of an external video signal.

Video-switch

Selection between internal video (pin 16) and external video (pin 13) is made by applying a switching potential to pin 18 (see Table 3). Video output (pin 20) from the device is filtered to remove the audio carrier and DC-coupled to pin 16. The TDA8304 provides the opportunity for a direct video connection (e.g. via a peritel connector) to be made to the device at pin 13. The AGC detector is not gated during the external video mode, the first phase detector is also not gated and operates with a short time constant. The gain of the

IF amplifier (in the external video mode) is reduced to prevent crosstalk of the video amplifier to the horizontal oscillator during the no-signal condition.

Horizontal synchronization

The horizontal synchronization circuit of the TDA8304 provides the drive pulse for a horizontal deflection stage.

- The phase of the control loop will be adapted automatically to the level of the input signal in order to achieve an optimum performance
- The control gradient of the control loop will be low at reception of weak signals to reduce the noise bandwidth.
- The phase detector control current is increased during strong or no-signal reception to obtain a short catching time and a good performance during VCR playback.

Vertical synchronization

The TDA8304 embodies a synchronized divider system for generating the vertical sawtooth at pin 3 having several advantages and features such as:

- The vertical frequency is alignment free. The divider automatically adapts to a vertical frequency of 50 Hz or 60 Hz including automatic amplitude correction and its operating modes offer maximum interference/disturbance protection.
- A discriminator-window checks the accuracy of the vertical trigger pulse. Internally clockpulses are generated by doubling the line frequency. The divider operates in the 60 Hz mode when the trigger pulse appears before count 576, otherwise the 50 Hz mode will be active.
- The divider system operates with a number of different reset windows. The windows are activated via an up/down counter. The counter increases its counter-value by 1 for each time the separated vertical sync pulse appears within the selected window, otherwise the counter value is lowered by 1.

Modes of operation

Large search window (divider ratio between 488 and 722). This mode is valid for the following conditions:

- Divider is looking for a new transmitter
- Divider ratio found does not comply with the narrow window specification limits
- Up/down counter value of the divider system, operating in the narrow window mode, drops below count 10

Narrow window mode: divider ratio between 522 - 528 (60 Hz) or 622 - 628 (50 Hz)

- The divider system switches over to narrow window mode when the up/down counter has reached his maximum value of 15 vertical sync pulses.
- When the divider operates in the narrow window mode and a vertical sync pulse is missing in the window, the divider is reset at the end of that window and the counter value is lowered by 1.
- At a counter value below 10 the divider system switches over to the large window mode.
- The divider system generate also the so-called anti-top-flutter pulse which inhibits the phase 1 detector during the vertical sync pulse. The width of this pulse depends on the divider mode. For the large window mode the start is generated at the reset of the divider. In the narrow window mode the anti-top-flutter pulse starts at the beginning of the first equalizing pulse. The anti-top-flutter pulse ends at count 10 for 50 Hz and at count 12 for 60 Hz.
- The divider is switched to count 625 when out of sync is detected by the coincidence detector. This results in a stable amplitude when no input signal is available.
- The divider is switched to the large window mode when enlarged vertical sync pulses are detected.

Table 1 AGC circuit operation

STATE	POSITIVE MODULATION	NEGATIVE MODULATION
input pin 32	HIGH/open	LOW

Table 2 AGC detector currents

STATE	POSITIVE MODULATION		NEGATIVE MODULATION	
action	current	condition	current	condition
charge	10 µA	V-sync signal	55 µA	-
charge	55 µA	pin 25 = LOW	-	-
discharge	3 mA	VITS signal	1.5 mA	H-sync signal

Table 3 Video switch operation

STATE	INTERNAL VIDEO	EXTERNAL VIDEO
input pin 18	LOW	HIGH

QUALITY SPECIFICATION

Quality level according to UZW-BQ/FQ-601.

SYMBOL	PARAMETER	RANGE A	RANGE B	UNIT
ESD	protection circuit specification (note 1)	2000	500	V
		100	200	pF
		1500	0	Ω

Note to the Quality specification

1. All pins of the IC are protected against ESD by means of the internal clamping diodes. Range A represents the human body model and range B represents the charge device model.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	supply voltage (pin 8)	-	13.2	V
P_{tot}	total power dissipation	-	2.3	W
T_{stg}	storage temperature range	−55	+150	°C
T_{amb}	operating ambient temperature range	−25	+65	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	TYP.	MAX.	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient in free air	30	35	K/W

The transmitter identification/coincidence detector

Pin 25 of the TDA8304 serves as the transmitter identification and/or coincidence detector (see Table 4). Pin 25 is HIGH (= 9.8 V) when a transmitter is present and LOW (= 0.3 V) when of no transmitter signal is detected. When the video switch is in the internal mode, the signal at the sync separator input (pin 28) is the demodulated IF signal, pin 25 will act as a coincidence detector. Pin 25 is HIGH when the horizontal oscillator loop is synchronized with the video signal and LOW in case of no synchronization. In the external video mode and in the text mode, pin 25 will be active as transmitter identification. The system relies upon the detection of sync pulses on the incoming IF signal. Pin 25 is charged with a current of 125 µA by the separated horizontal sync pulse and discharged continuously with a current of 4 µA. The high impedance of pin 25 should be taken into account in the application concept.

The 50/60 Hz identification

The 50/60 Hz information (see Table 5) derived from the divider system is available at the open collector output pin 14.

Table 4 Transmitter identification/coincidence detector

STATE	INTERNAL VIDEO					EXTERNAL VIDEO	
input pin 18	LOW					HIGH	
input pin 12	TV mode = HIGH		Text mode = LOW				
Input signal pins 9 and 10	yes	none	yes	none	none	yes	none
input pin 28	50/60 Hz	none	50/60 Hz	VCS text	none	don't care	don't care
output pin 25	9.8 V	0.3 V	9.8 V	0.3 V	0.3 V	9.8 V	0.3 V

Table 5 50/60 Hz identification

INPUT/OUTPUT	STATUS	STATUS	STATUS
Input signal pins 9 and 10	don't care	don't care	don't care
input pin 28	50 Hz	60 Hz	none
output pin 14	0.3 V	12 V	0.3 V

CHARACTERISTICS

T_{amb} = 25 °C;V_p = 12 V; carrier 38.9 MHz negative modulation, unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply (pin 8)						
V_8	supply voltage range		10	12	13.2	V
I_8	supply current	no input	90	115	140	mA
I_{12}	start current (pin 12)	note 1	-	6.5	9	mA
V_{12}	start protection level	I_{12} = 12 mA	-	-	16.5	V
IF Amplifier						
$V_{9-10(rms)}$	input sensitivity (RMS value)	note 2	25	40	65	µV
R_{9-10}	differential input resistance	note 3	-	1300	-	Ω
C_{9-10}	differential input capacitance	note 3	-	5	-	pF
G_{9-10}	gain control range		-	74	-	dB
ΔV_{20}	output signal expansion for 46 dB input signal variation	note 4	-	1	-	dB
V_{9-10}	maximum input signal		100	170	-	mV
$V_{9-10(rms)}$	input sensitivity in external mode (RMS value)	note 2	250	400	650	µV
Video Amplifier (notes 5 and 6)						
V_{20}	negative modulation, zero signal level		4.7	4.9	5.1	V
V_{20}	positive modulation, zero signal level		2.5	2.7	2.9	V
V_{20}	peak sync (negative modulation)	note 7	2.5	2.75	3.0	V
V_{20}	white level (positive modulation)	note 7	4.7	4.9	5.1	V
V_{20}	white spot threshold level		-	5.7	-	V
V_{20}	white spot insertion level		-	4	-	V
Z_{20}	video output impedance		-	25	-	Ω
I_{20}	internal bias current of npn emitter follower output transistor		1.4	1.8	-	mA
I_{source}	maximum source current (pin 20)		10	-	-	mA
B	bandwidth of demodulated output signal		5	6	-	MHz
G_{20}	differential gain	note 8	-	2	5	%
φ	differential phase	note 8	-	2	5	deg
NL	video non-linearity	note 9	-	2	5	%
	intermodulation	note 10				
	1.1 MHz; blue		50	60	-	dB
	1.1 MHz; yellow		50	60	-	dB
	3.3 MHz; blue		55	65	-	dB
	3.3 MHz; yellow		55	65	-	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
S/N	signal-to-noise ratio	10 mV input signal	52	58	-	dB
		end of gain control range; note 11; see Fig.5	57	62	-	dB
V_{20}	residual carrier signal		-	2	10	mV
V_{20}	residual 2nd harmonic of carrier signal		-	2	10	mV
System switch (note 12)						
AGC ON PEAK SYNC LEVEL FOR NEGATIVE MODULATION SIGNALS						
V_{32}	control voltage		0	-	0.8	V
I_{32}	input current		−100	-	−500	µA
AGC ON WHITE LEVEL FOR POSITIVE MODULATION SIGNALS						
V_{32}	control voltage		2	-	12	V
I_{32}	input current		0	-	1	mA
IF sync separator						
I_I	input current		0.4	0.6	0.8	mA
I_O	output current (pin 1)		22	27	32	µA
V_I	clamp level		-	3.3	-	V
Tuner AGC						
$V_{9\text{-}10(rms)}$	minimum starting point for tuner take-over (RMS value)		-	-	0.2	mV
$V_{9\text{-}10(rms)}$	maximum starting point for tuner take-over (RMS value)		100	150	-	mV
I_6	maximum tuner AGC output swing	V_6 = 3 V	4	-	-	mA
V_6	output saturation voltage	I_6 = 2 mA	-	-	300	mV
I_6	leakage current		-	-	1	µA
	input signal variation complete tuner control	ΔI_6 = 2 mA	0.2	2	4	dB
V_2	minimum voltage tuner take-over		-	-	1	V
AGC detection level						
I_{17}	charge current		-	200	-	µA
I_{17}	discharge current		-	20	-	µA
V_{17}	clamp level		-	2.9	-	V
Video switching circuit (note 13)						
EXTERNAL POSITIVE VIDEO INPUT						
$V_{13(p\text{-}p)}$	input signal (peak-to-peak value)	V_O = 2.5 V(p-p)	-	1	-	V
I_{13}	input current		-	1.5	5	µA
V_{13}	peak sync clamping level	I_{13} = 1 mA	1.65	1.85	2.05	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
INTERNAL VIDEO INPUT						
$V_{16(p-p)}$	Internal video input signal (peak-to-peak value	V_O = 2.5 V(p-p)	-	2	-	V
I_{16}	input current		-	1.5	5	µA
V_{16}	noise clamping level	I_{16} = 1 mA	2.2	2.4	2.6	V
VIDEO OUTPUT (POSITIVE VIDEO)						
$V_{15(p-p)}$	video output signal (peak-to-peak value)		2.3	2.5	2.7	V
V_{15}	peak sync signal		-	3	-	V
I_{bias}	internal bias current (pin 15)		1	1.5	-	mA
I_O	maximum output current (pin 15)		5	-	-	mA
α	crosstalk external to internal	notes 14 and 24	-	55	-	dB
α	crosstalk internal to external	notes 14 and 24	-	55	-	dB
Video switch						
V_{18}	input voltage for internal video		-	-	0.8	V
V_{18}	input voltage for external video		2	-	V_P	V
I_{18}	maximum current	V_{18} = 0 V	-	0.05	0.2	mA
		V_{18} = 12 V	-	0.25	1	mA
Text/TV switch						
V_{12}	input voltage for text mode		-	-	0.8	V
V_{12}	input voltage for TV mode		2	-	V_P	V
I_{12}	maximum current	V_{12} = 0 V	-	-	0.3	mA
		V_{12} = 11.5 V	-	-	1.5	mA
AFC-circuit (note 15)						
I_{22}	AFC sample and hold switch-off current		0.1	-	-	mA
I_O	output current (pin 22)	V_{22} = 0 V	0.2	0.4	0.8	mA
I_{LI}	leakage current (pin 22)		-	-	1	µA
V_{21}	AFC output voltage swing		10.5	-	11.5	V
I_{21}	available output current		±0.2	-	-	mA
	control slope		-	100	-	mV/kHz
V_O	output voltage (pin 21)	AFC off	5.5	6	6.5	V
R_O	AFC output resistance		-	40	-	kΩ
$V_{21(p-p)}$	output voltage swing	notes 16 and 24	-	11	-	V
	control slope	notes 16 and 24	-	80	-	mV/kHz
V_{21}	output voltage shift with respect to V_I = 10 mV(RMS)	notes 16 and 24	-	−2	-	V
Sync separator (see Fig.6)						
V_{28}	required sync pulse amplitude	note 17	200	750	-	mV
I_{28}	input current	V_{28} > 5 V	-	8	-	µA
		V_{28} = 0 V	-	−10	-	mA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
First control loop						
Δf	PLL holding range		-	±1500	±2000	Hz
Δf	PLL catching range		±600	±1500	-	Hz
	control sensitivity to oscillator	note 18	see Fig.7			
$V_{9\text{-}10(rms)}$	IF input signal for switching from fast to slow (RMS value)		-	2.2	-	mV
Second control loop (positive edge)						
$\frac{\delta t_d}{\delta t_o}$	control sensitivity, see Fig.6	note 19	-	100	-	
t_d	control range		-	25	-	µs
Phase adjustment (via second control loop)						
	control sensitivity		-	25	-	µA/µs
α	maximum allowed phase shift		-	±2	-	µs
Horizontal oscillator						
	free running frequency	R = 34.3 kΩ; C = 2.7 nF	-	15625	-	Hz
Δf	spread with fixed external components		-	-	4	%
Δf	frequency variations with supply voltage from 10 to 13.2 V		-	-	2	%
Δf_T	frequency variation with temperature	note 24	-	−1.6	-	Hz/°C
Δf_{fr}	maximum frequency deviation at start of horizontal output		-	-	10	%
Δf	frequency variation when only noise is received	note 24	-	-	500	Hz
Horizontal output (open collector; pin 29)						
V_{29}	output limiting voltage		-	-	16.5	V
V_{OL}	output voltage LOW	I_{sink} = 10 mA	-	0.3	0.5	V
I_{sink}	maximum sink current		10	-	-	mA
	duty factor of output signal		-	46	-	%
t_r	rise time output pulse		-	260	-	ns
t_f	fall time output pulse		-	100	-	ns
Flyback input and sandcastle output (note 20)						
I_{30}	required input current during flyback pulse		0.1	-	2	mA
V_{30}	output voltage during burstkey horizontal blanking vertical blanking		 8 4 2.1	 - 4.4 2.5	 - 5 2.9	 V V V
t_W	pulse width of burstkey at 60 Hz signals at 50 Hz signals		 2.9 3.2	 3.3 3.6	 3.7 4	 µs µs

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Flyback input and sandcastle output (note 20)						
	width of horizontal blanking pulse		flyback pulse width			
	width of vertical blanking pulse divider in search window divider in narrow window	 50 Hz 60 Hz 50 Hz 60 Hz	 - - - -	 21 17 25 21	 - - - -	 lines lines lines lines
t_d	delay between the start of the sync pulse at the video output and the burstkey pulse trailing edge rising edge	60 Hz	 - 4.7	 - 5.4	 9.3 6.1	 µs µs
Vertical ramp generator (note 22)						
I_3	input current during scan		-	-	2	µA
I_3	discharge current during retrace		-	0.8	-	mA
$V_{3(p-p)}$	sawtooth amplitude (peak-to-peak value)		-	1.9	-	V
t	interlace timing of the internal pulses	note 24	30	32	34	µs
Vertical output						
I_4	available output current	V_4 = 4 V	-	-	3	mA
V_4	maximum available output voltage	I_4 = 0.1 mA	4.4	5	-	V
Vertical feedback input						
V_5	DC input voltage		2.9	3.3	3.7	V
$V_{5(p-p)}$	AC input voltage (peak-to-peak value)		-	1	-	V
I_5	input current		-	-	12	µA
	internal pre-correction to sawtooth		-	3	-	%
	deviation amplitude 50/60 Hz		-	-	2	%
	temperature dependency of the amplitude	note 24 ΔT = 45 °C	-	-	2	%
Vertical guard						
ΔV_5	active switch level at a deviation with respect to the DC feedback level guard level LOW guard level HIGH	note 23; V_{30} = 2.5 V	 - -	 1.5 2	 - -	 V V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Coincidence detector/transmitter identification (note 21)						
V_{25}	voltage for in-sync condition		-	9.8	-	V
V_{25}	voltage for no-sync condition	no signal	-	0.3	-	V
V_{25}	switching level to switch the phase detector from fast to slow		6.2	6.7	7.2	V
V_{25}	hysteresis slow to fast		-	0.6	-	V
V_{25}	switching level to activate the mute function (transmitter identification)		2.5	2.8	3.1	V
V_{25}	hysteresis mute function		-	2.0	-	V
I_{25}	load (allowed) at pin 25		–2	-	2	µA
50/60 Hz identification (open collector output)						
V_{14}	output voltage at 50 Hz (no signal)		-	0.3	0.5	V
V_{14}	output voltage at 60 Hz		-	V_p	-	V
I_{14}	sink current active		-	-	5	mA
I_{14}	output current inactive (transmitter present)		-	-	1	µA

Notes to the characteristics

1. Supplying a current of 9 mA to pin 12 starts the horizontal oscillator. This current can be obtained via a bleed circuit from the mains rectifier whilst the main supply for the device (V_{cc}) is obtained from the horizontal output stage. The load current of the driver must be added to the value given.
2. On set AGC.
3. The input impedance has been chosen such that a SAW filter can be employed.
4. Measured with 0 dB = 450 µV.
5. Measured at 10 mV RMS 100% input signal.
6. Projected zero point; i.e. with switched demodulator.
7. The output signal amplitude is determined by the AGC detector. For negative modulation the peak sync level is used as reference. With positive modulation the white level is stabilized.
8. Measured according to the test line given in Fig. 3. The differential gain is expressed as a percentage of the difference in peak amplitudes between the largest and smallest value relative to the subcarrier amplitude at blanking level. The differential phase is defined as the difference in degrees between the largest and smallest phase angle. The differential gain and phase are measured with a DSB signal.
9. This figure is valid for the complete video signal amplitude (peak white-to-black). The non-linearity is expressed as a percentage of the maximum deviation of a luminance step from the mean step, with respect to the mean step.
10. The test set-up and input conditions are given in Fig. 5. The figures are measured at an input signal of 10 mV RMS.
11. Measured with a source impedance of 75 Ω.

$$\textit{The signal-to-noise ratio} = 20 \log \frac{V_o \ \textit{black-to-white}}{V_{n(rms)} \ \textit{at} \ B = 5 \ \textit{MHz}}$$

12. By means of the system switch 2 conditions can be obtained. Negative modulation with peak sync level AGC. This is obtained with pin 32 connected to ground. Positive modulation with peak white AGC. This is obtained with pin 32 connected to the positive supply.

13. When the video switch is in the external mode the first control loop in the synchronization circuit is not switched to a long time constant when weak signals are received.
14. Defined as 20 log $\frac{V_O \textit{ unwanted video black-to-white}}{V_O \textit{ wanted video-black-to-white}}$; measured at 4.4 MHz.
15. The indicated figures are measured at an input signal of 10 mV RMS. The unloaded Q-factor of the reference tuned circuit is 70. With very weak input signals the drive signal for the AFC circuit will have a high noise content. This noise input has a asymmetrical frequency spectrum which will cause an offset of the AFC output voltage. To avoid problems due to this effect a notch filter can be built into the demodulator tuned circuit. The characteristics given for weak signals are measured without a notch circuit, with a SAW filter connected in front of the IC input signal such that the input signal of the IC is 150 μV (RMS value).
16. Measured at an input signal amplitude of 150 μV(RMS) (pin 21).
17. The minimum value is obtained by connecting a 1.8 kΩ resistor between pins 15 and 28. The slicing level can be varied by changing the value of this resistor (higher resistor value results in larger value of the minimum sync pulse amplitude). The slicing level is independent of the video information.
18. Frequency control is obtained by supplying a correction current to the oscillator RC network via a resistor connected between the phase 1 detector output and the oscillator network. The oscillator can be adjusted to the correct frequency by short circuiting the sync separator bias network (pin 28) to $+V_p$. To avoid the need of a VCR switch the time constant of the phase detector at strong input signals is sufficiently short to get a stable picture during VCR playback. During the vertical retrace period the time constant is even shorter so that the head-errors of the VCR are compensated at the beginning of scan. During conditions of weak signal (information derived from the AGC circuit) the time constant is increased to obtain a better noise immunity.
19. This figure is valid for an external load impedance of 82 kΩ from pin 31 to the phase adjustment potentiometer (of H-shift).
20. The flyback input and sandcastle output have been combined on one pin. The flyback pulse is clamped to a level of 4.5 V. The minimum current to drive the second control loop is 0.1 mA.
21. The functions in-sync/out-of-sync and transmitter identification have been combined on this pin. The capacitor is charged during the sync pulse and discharged during the time difference between gating (6.5 μs) and the sync pulse in the internal video mode. When the circuit is in the external mode the capacitor is charged by the horizontal sync pulse and discharged continuously with a small current.
22. The vertical scan is synchronized by means of a divider system. Therefore no adjustment is required for the ramp generator. The divider detects whether the incoming signal has a vertical frequency of 50 or 60 Hz and corrects the vertical amplitude.
23. To avoid screen burn due to a collapse of the vertical deflection a continuous blanking level (V_{30} = 2.5 V) is inserted in the sandcastle pulse when the feedback voltage of the vertical deflection is not within the specified limits.
24. These figures are based on test samples.

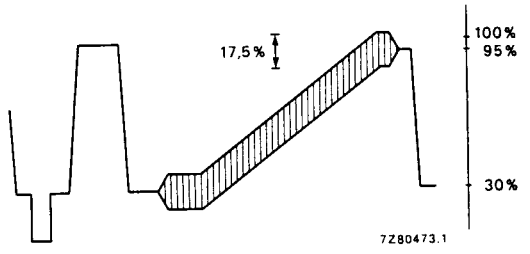


Fig.2 Video output signal.

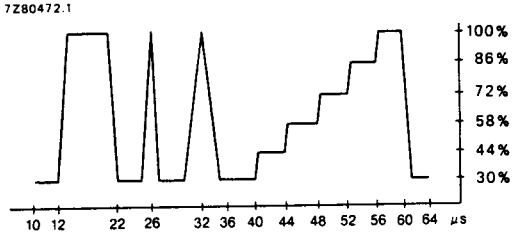
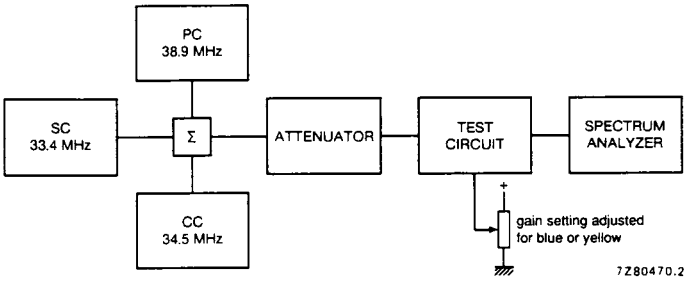
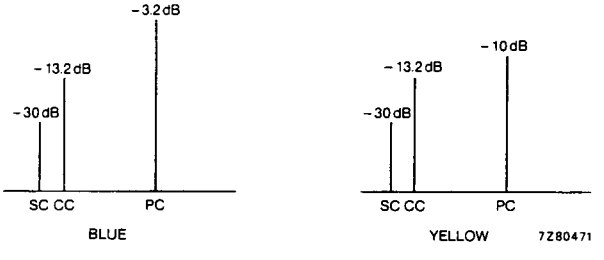


Fig.3 EBU test signal waveform (line 17).





Input signal conditions

SC = Sound carrier

CC = Chrominance carrier

PC = Picture carrier

All with respect to peak sync level

$$Value\ at\ 1.1MHz : 20 \log \frac{V_o\ at\ 4.4MHz}{V_o\ at\ 1.1MHz} + 3.6dB$$

$$Value\ at\ 3.3MHz : 20 \log \frac{V_o\ at\ 4.4MHz}{V_o\ at\ 3.3MHz}$$

Fig.4 Test set-up intermodulation.

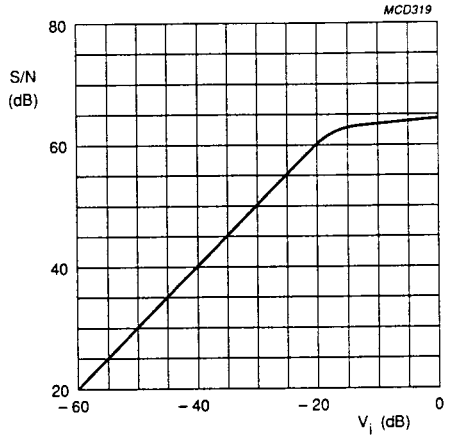
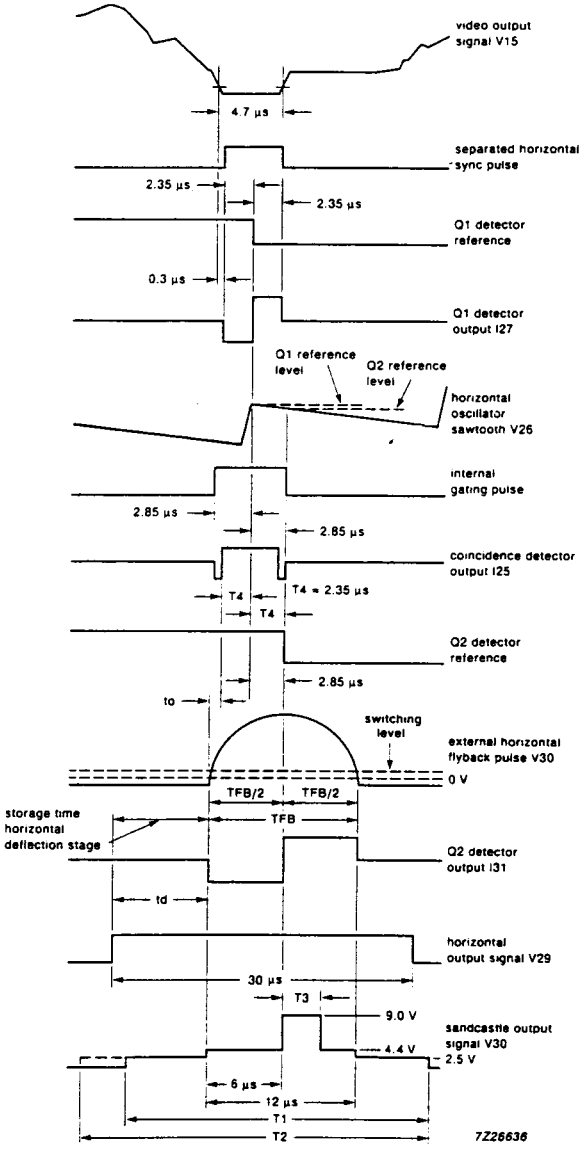


Fig.5 Signal-to noise ratio as a function of the input voltage (0 dB = 100 mV).



T1: divider in search window: 42p (50 Hz); 34p (60 Hz); $p = 1/2f_H$

T2: divider in narrow window: 50p (50 Hz); 42p (60 Hz)

T3: 3.6 µs (50 Hz); 3.3 µs (60 Hz)

Fig.6 Timing diagram.

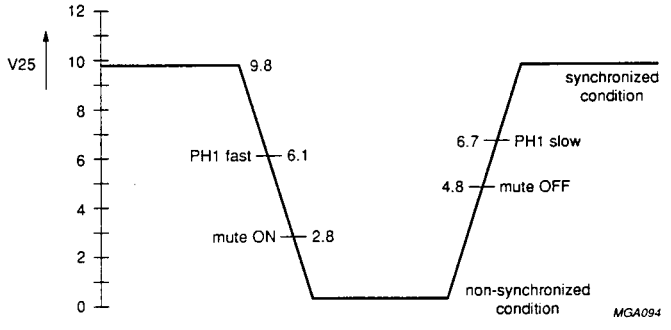


Fig.7 Switching levels coincidence detector.

CONDITION PIN 18 VIDEO SWITCH	CONDITION V_{25}	CONTROL SENSITIVITY HOR.OSCILLATOR kHz / µs	
		T2 - T1	T3 = SCAN
Low internal video	V_{25} > 6.7 V and strong signal	11.3	7.6
	V_{25} > 6.7 V and weak signal	1.3	1.3
	V_{25} < 6.1 V and strong signal	11.3	7.6
	V_{25} < 6.1 V and weak signal	11.3	7.6
HIGH or floating external video	don't care	11.3	7.6

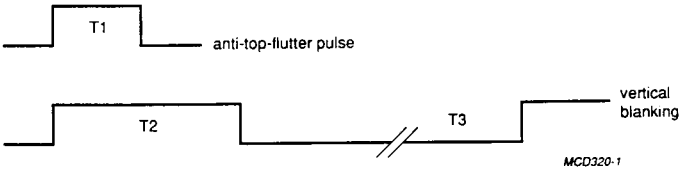


Fig.8 Anti-top-flutter-pulse.

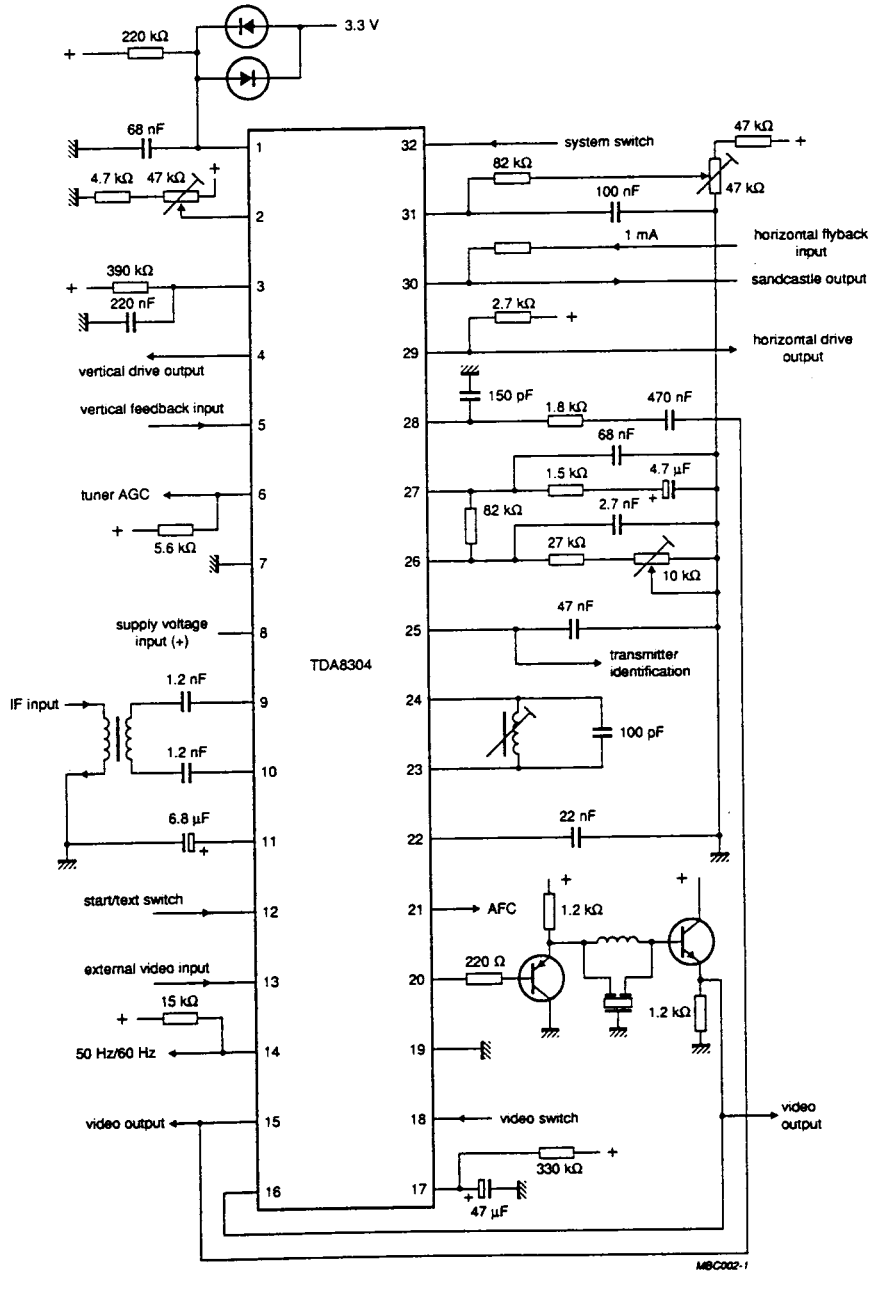


Fig.9 Application diagram.