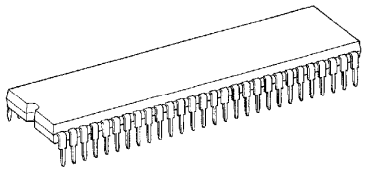
TOSHIBA BIPOLAR LINEAR INTEGRATED CIRCUIT SILICON MONOLITHIC

TA8725AN

1CHIP COR NTSC CTV

The TA8725AN combines all the functions required for an NTSC CTV system in a 56-lead, dual-in-line shrink-type plastic package.
This IC includes PLL type PIF / SIF circuits, video / chroma / deflection circuits and OSD interfaces.



SDIP56-P-600-1.78

Weight : 5.55g (Typ.)

FEATURES

PIF stage

- Split carrier PLL type PIF
- High speed 3-stage variable gain PIF amplifier with dual time constants (Peak AGC)
- Single-end AFT output with defeat function
- RF AGC output (Reverse AGC)
- Sync. negative detected video output
- Internal black / white noise inverter with EIA decoder SW (for IS-15)

SIF stage

- Split carrier SIF
- 20dB SIF AGC
- Quadrature FM detector circuit with sound mute function

Video stage

- Black expander
- Variable DC restoration ratio
- Built-in video delay-line with 3.58MHz trap
- Picture sharpness with internal delay-line (160ns)
- Contrast control with uni-color function
- Brightness control

Chroma stage

- Built-in take off or 3.58MHz Band-pass filters can be selected.
- Built-in ACC and killer filters
- Color control
- Tint control
- Color differential outputs
- Filter automatic tuning

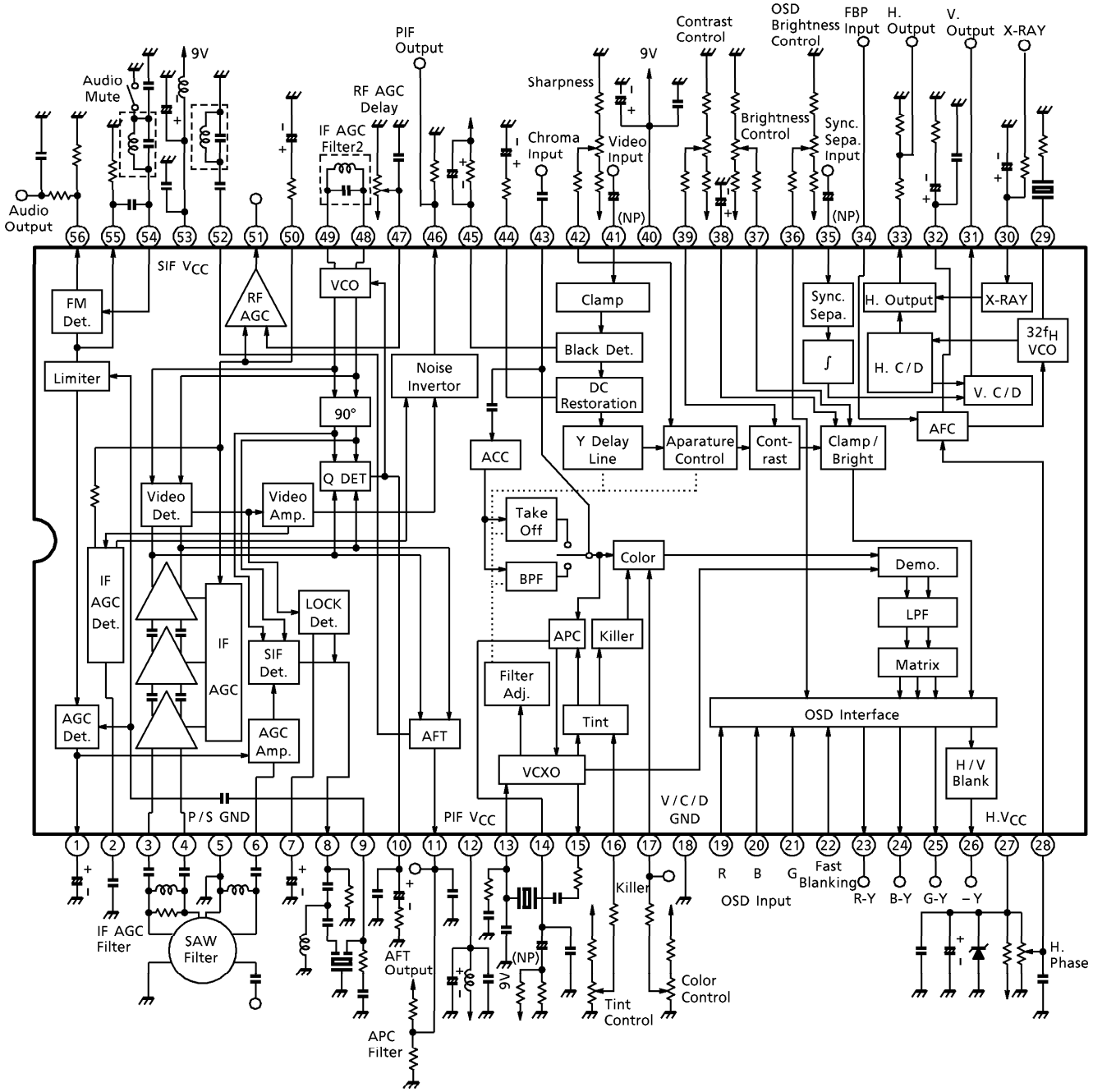
Detection stage

- Adjustment-free horizontal and vertical count down system
- Built-in vertical integral and V. sepa. circuit
- Vertical drive pulse output for TA8445K
- X-ray protect circuit

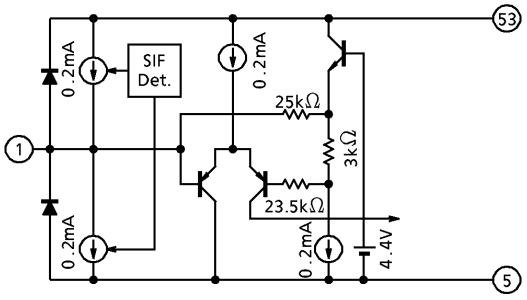
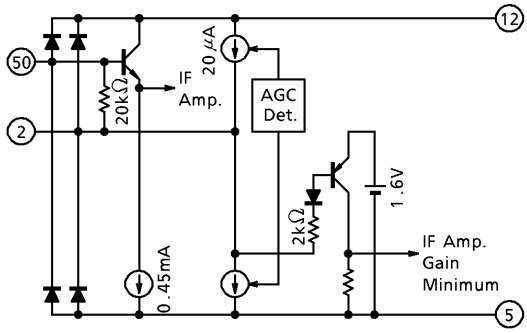
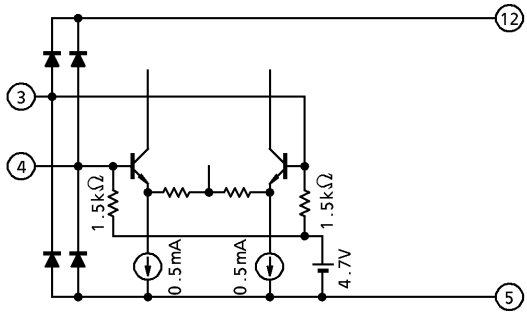
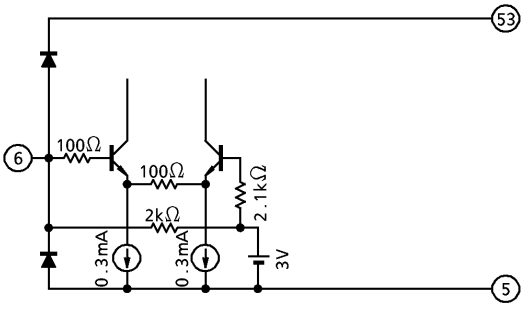
OSD interface stage

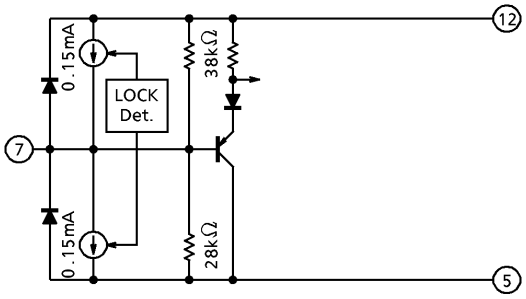
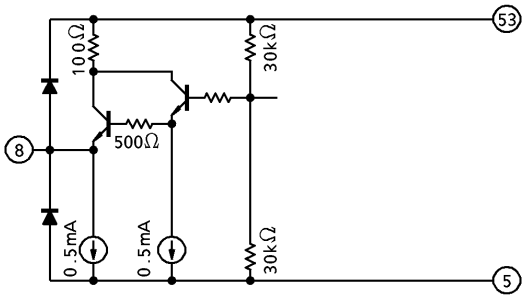
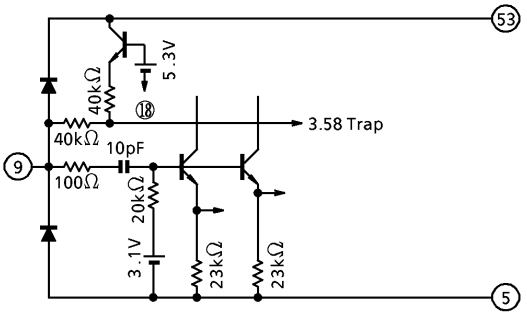
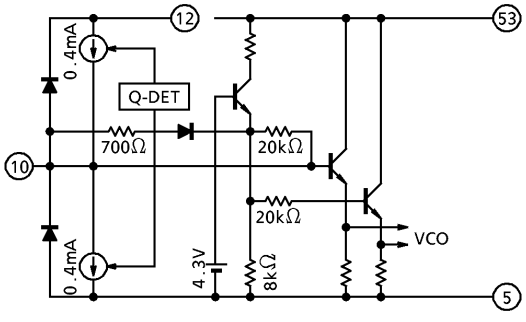
- R, G and B OSD input
- Fast-blanking SW input
- OSC brightness control

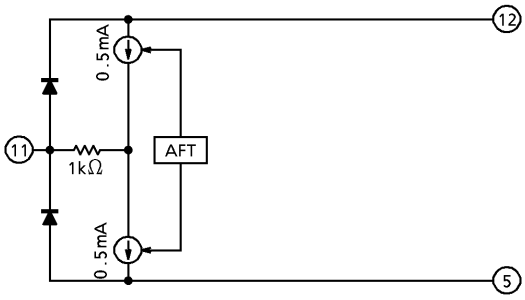
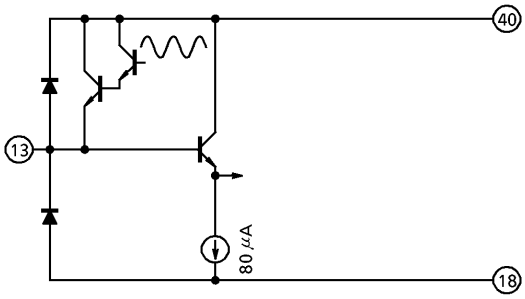
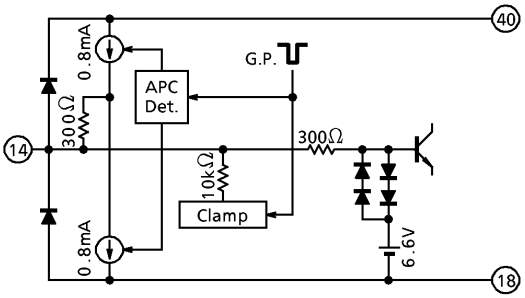
BLOCK DIAGRAM

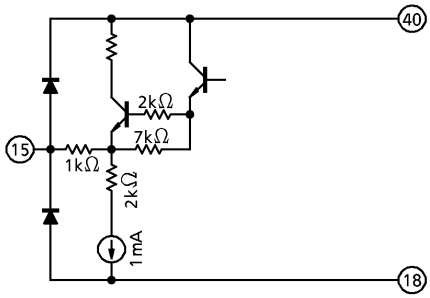
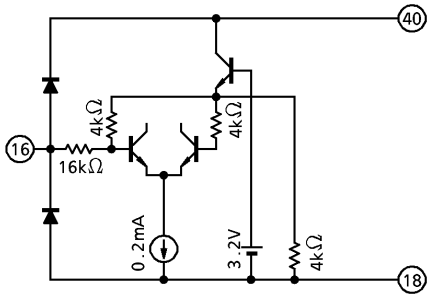
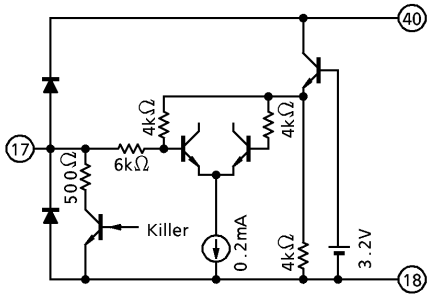
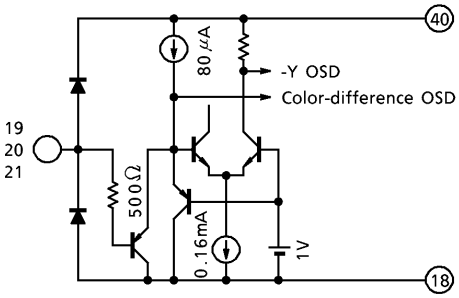


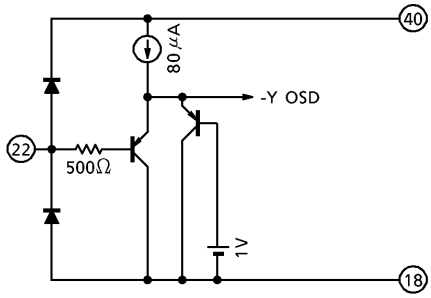
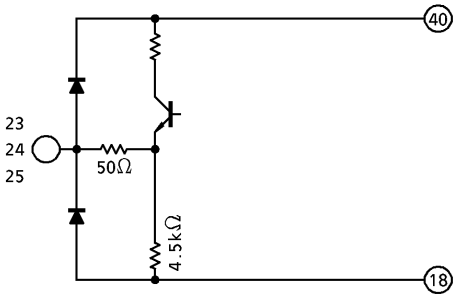
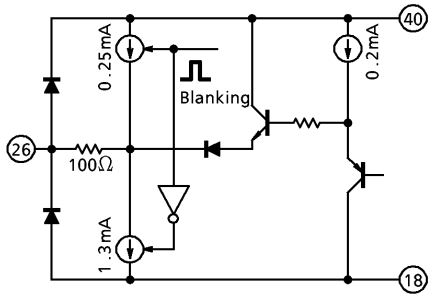
TERMINAL FUNCTION

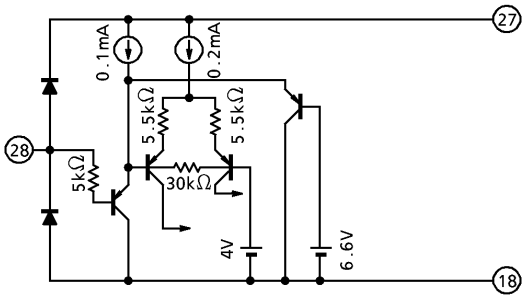
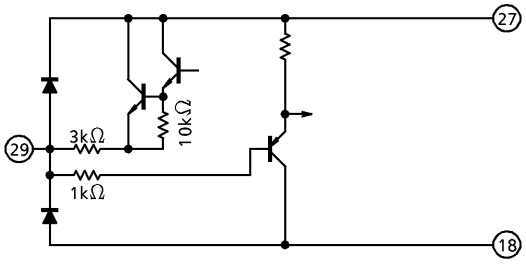
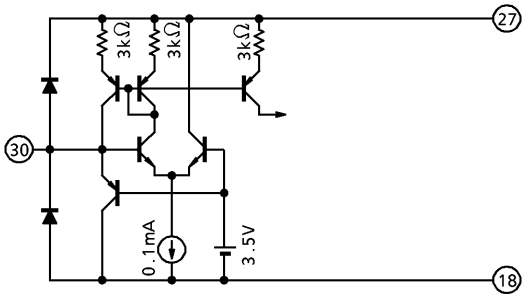
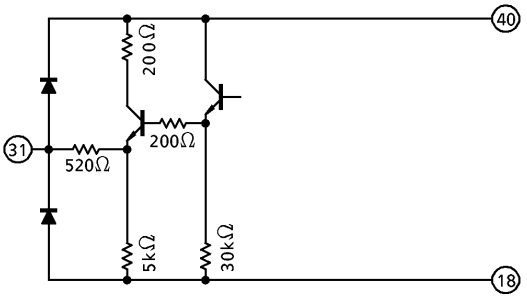
PIN No.	PIN NAME	FUNCTION	INTERFACE CIRCUIT
1	SIF AGC	This is a SIF AGC filter terminal. AGC is applied in the SIF input stage. This AGC is referenced to the limiter input signal.	
2	1st AGC	This is a PIF 1st AGC filter terminal. Peak AGC is applied in the PIF 3-stage amp. This AGC is referenced to the PIF-detection output signal after the video amp. A high-speed AGC circuit based on dual time constants is used here. By connecting this pin to GND, requirements under the U.S. IS-15 standards can be met.	
3 4	PIF Input 1 PIF Input 2	This is a PIF differential amp. input pin. A 3-stage, dual-time constant, high-speed AGC amp. is incorporated here. The standard PIF input level is 84dBμV.	
5	P/S GND	This is a GND pin for the PIF and SIF circuits.	—
6	SIF Input	This is a SIF amp. input pin. An AGC amp. with a gain variable range of approx. 20dB is incorporated here. The standard SIF input signal level is 75dBμV. The AGC response range is −10dB.	

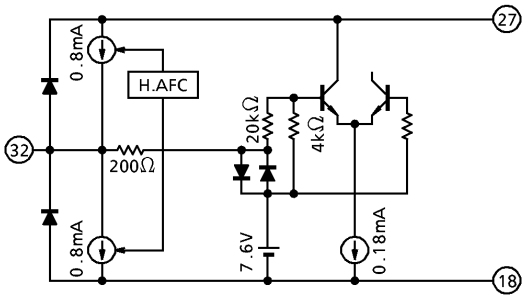
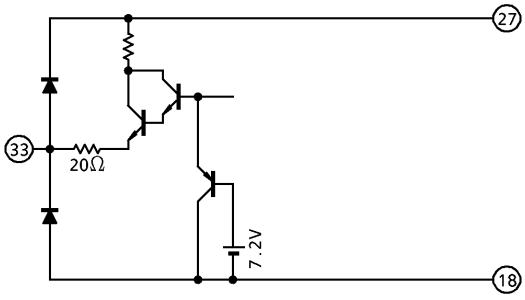
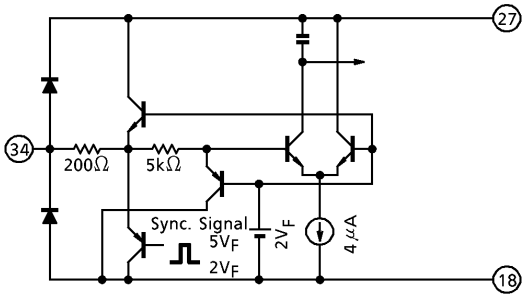
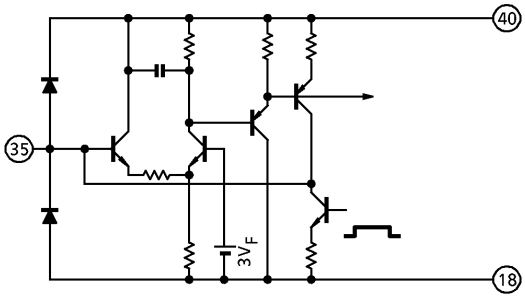
PIN No.	PIN NAME	FUNCTION	INTERFACE CIRCUIT
7	PLL Sync. Det.	This is a PLL sync. Det. filter terminal. The PLL synchronization is detected by identifying whether or not signal is present after meanvalue-demodulating the PIF-Det. output signal. The result of sync. Det. is output from the SIF output pin as a DC voltage. When locked in phase : HIGH level When not locked in phase : LOW level	
8	SIF Output	This is a SIF-Det. output pin. Make sure that the output from this pin is fed to the limiter input terminal through a 4.5MHz band-pass filter. This pin also functions as a PLL sync. Det. output pin. Check the DC voltage from this pin to see the locked condition of the PLL circuit. The DC voltage is as follows : When locked in phase : HIGH level When not locked in phase : LOW level	
9	Limiter Input	This is a limiter amp. input pin. Use this pin to input an audio FM modulation signal. AGC control is applied using the SIF amp. to maintain the limiter amp. input signal level at about 100dBμV. This pin also functions as a chroma trap switch in the video section. LOW level : ON HIGH level : OFF	
10	Loop Filter	This is a PIF PLL loop filter terminal. This terminal contains a circuit to select the desired loop filter time constant during PLL sync. Det.	

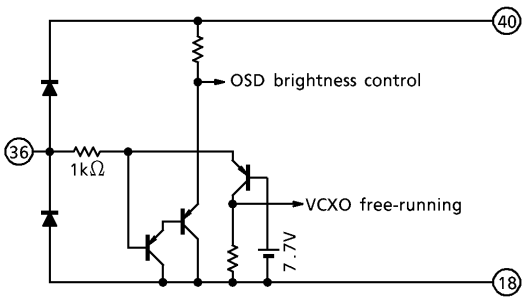
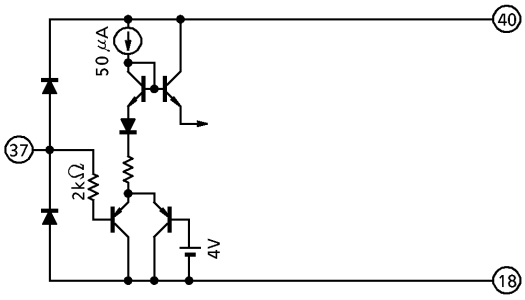
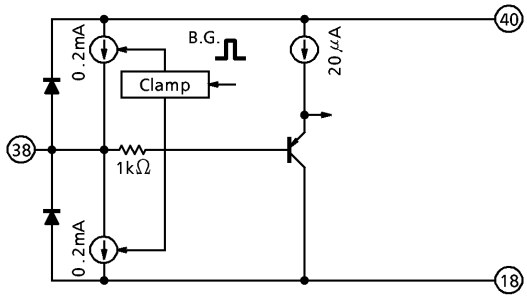
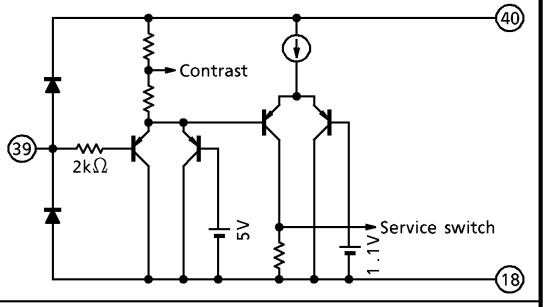
PIN No.	PIN NAME	FUNCTION	INTERFACE CIRCUIT
11	AFT Output	This is an AFT output pin. The AFT output is monopolarity. The AFT function can be muted by driving the AFT tank pin LOW.	
12	PIF V_{CC}	This is a PIF circuit V_{CC} pin. It is recommended that a trap for the PIF carrier frequency be inserted in series to prevent characteristics degradation due to current leakage from V_{CC}. (In the applications circuit example, a 68μH coil is inserted.) V_{CC} = 9V (Typ.)	—
13	VCXO Input	Connect a crystal resonator-based resonance circuit between this pin and the VCXO drive pin to configure a color sub-carrier oscillator circuit. Although APC is applied to the burst signal when the chroma signal is input, VCXO becomes a free-running oscillator by connecting the OSD brightness control pin to V_{CC} with 100.	
14	APC Filter	This is an APC filter terminal for color sub-carrier PLL. APC is applied to ensure that the burst signal of chroma input is phase-locked to the VCXO oscillator output signal.	

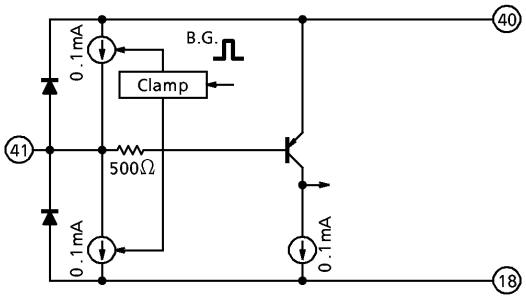
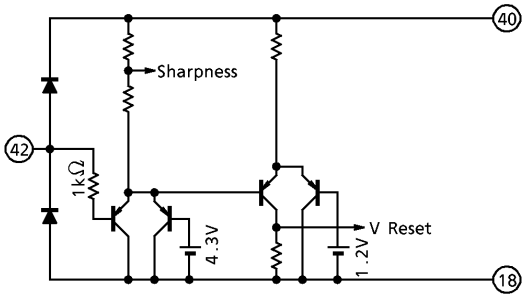
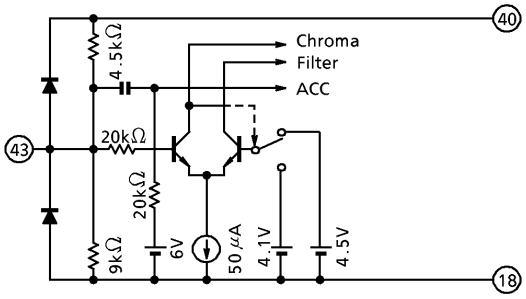
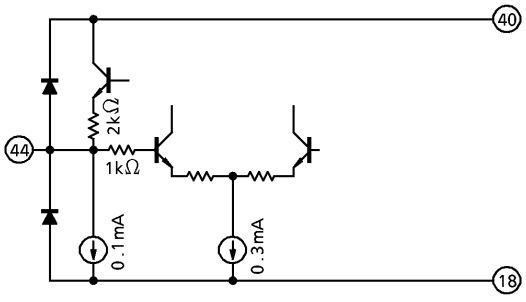
PIN No.	PIN NAME	FUNCTION	INTERFACE CIRCUIT
15	VCXO Drive	Connect a crystal resonator-based resonance circuit between this pin and the VCXO input pin to configure a color sub-carrier oscillator circuit. Because the VCXO oscillator output signal is referenced to by the built-in filter automatic adjustment circuit, it is necessary that the VCXO free-running frequency be adjusted to 3.579545MHz by using an external time constant.	
16	Tint Control	This is a Tint control pin. The tint can be adjusted +55° by using DC voltages of 1 to 4V. An APC tint circuit is used here.	
17	Color Control	This is a color control pin. The color gain can be adjusted 40dB by using DC voltages of 1 to 4V. When the killer circuit turns on, the voltage on this pin is pulled LOW to turn off the color-difference output. When connected to V_{CC} with 2.2kΩ, this pin can be used to observe the chroma filter output signal.	
18	V/C/D GND	This is a GND pin for the video, chroma and deflection circuits.	—
19 20 21	OSD R OSD B OSD G	These are R, B and G OSD input pins. When OSD is ON, the color-difference output for that color is set to 6.9V, and other color-difference outputs are set to 5.4V. The -Y output generates a DC voltage that is determined by the voltage on the OSD brightness control pin during that time. The OSD-ON threshold voltage is 1.0V. OSD is ON when the voltage is HIGH or open : OSD is OFF when the voltage is LOW.	

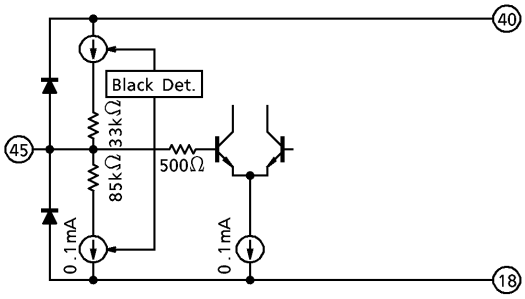
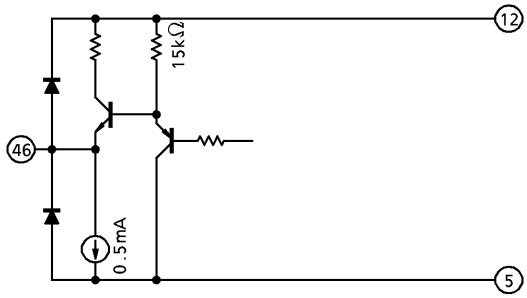
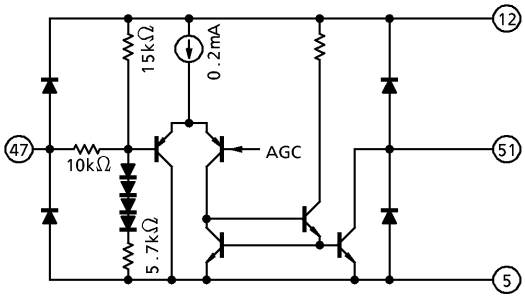
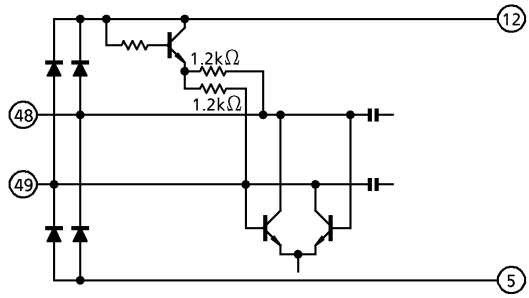
PIN No.	PIN NAME	FUNCTION	INTERFACE CIRCUIT
22	Fast Blanking Input	This is a fast blanking input pin. When OSD is ON, the color-difference output generates 5.4V, and the -Y output generates a DC voltage that is determined by the voltage on the OSD brightness control pin during that time. The OSD-ON threshold voltage is 1.0V. OSD is ON when the voltage is HIGH or open : OSD is OFF when the voltage is LOW. OSD R, B and G are given priority.	
23 24 25	R-Y Output B-Y Output G-Y Output	These are color-difference output pins. The minimum load resistance these outputs can drive is 2.5kΩ.	
26	-Y Output	This is a -Y output pin. Vertical blanking is disabled by connecting the OSD brightness control pin to V_{CC} with 100Ω. The minimum load resistance this output can drive is 3.5kΩ.	
27	H.V_{CC}	This is a V_{CC} pin for the horizontal sync. circuit. Because a large current flows in the horizontal output circuit, make sure that the impedance of the wiring patterns, etc. is sufficiently small and that the bypass capacitors are sufficiently strong. H.V_{CC} = 6.8V (Typ.)	—

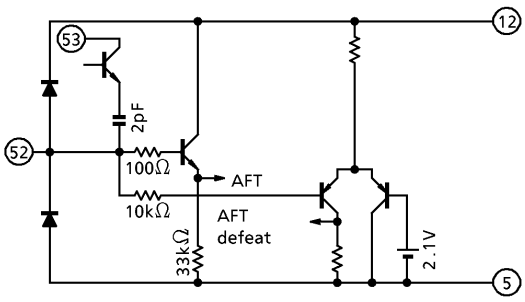
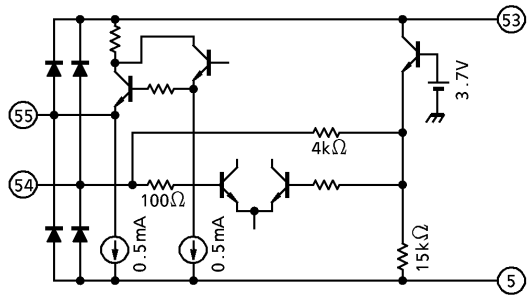
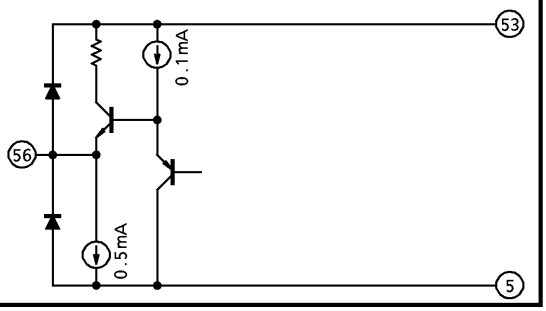
PIN No.	PIN NAME	FUNCTION	INTERFACE CIRCUIT
28	H. Phase Adjustment	This is a horizontal phase control pin. The horizontal phase can be adjusted $-1\mu s$ by using a DC voltage from GND to H.V_{CC}. Use this function to adjust the offset of the horizontal screen position.	
29	32f_H VCO	Connect a 32f_H ceramic filter to this pin. Because the horizontal sync. and vertical sync. circuits use a count-down system. no adjustments are required for these sync. circuits.	
30	X-RAY	This is an overvoltage protection input pin. When the voltage applied to this pin is 3.5V or more, the horizontal oscillator output is turned off, and the chip is placed in an overvoltage-protected state (pin voltage = 4.2V). The protected state is cleared when a holding current of 100 is absorbed from an external source. Connect a bypass capacitor of about 10μF to prevent erratic operation caused by pulse leakage from the vertical output pin or inclusion of external noise.	
31	V. Output	This is a vertical pulse output pin. This pin outputs a TTL-level, 10H-wide pulse of the positive polarity. Connect this pin to a pulse input type of vertical output IC. (e.g., the TA8445K) The vertical oscillator circuit uses a count-down system : when an off-standard signal is input, it oscillates at 60Hz. The minimum load resistance this output can drive is 4.1kΩ.	

PIN No.	PIN NAME	FUNCTION	INTERFACE
32	AFC Filter	This is an AFC filter terminal for the horizontal oscillator PLL. AFC is applied using the sync. signal and FBP to control the $32f_H$ VCO oscillator.	
33	H. Output	This is a horizontal output pin. Its duty cycle is 37.5%. The minimum load resistance this output can drive is 500Ω.	
34	FBP Input	This is a FBP input pin. This signal is referenced to when generating the horizontal AFC, gate pulse, and horizontal blanking. Because a sync. separation output is superimposed on the pulse as it is input to this pin. this input can be used for the microcomputer to determine whether or not a signal is present. The FBP width is 12μs (Typ.)	
35	Sync. Sepa. Input	This is a horizontal / vertical sync. separation input pin. The horizontal sync. is separated as the input coupling capacity is charged and discharged, and the vertical sync. is separated as the built-in capacity is charged and discharged. The continuity of the vertical sync. separation signal is checked to determine whether standard or not. The sync. separation level is Horizontal sync. : 30% Vertical sync. : 35%	

PIN No.	PIN NAME	FUNCTION	INTERFACE CIRCUIT
36	OSD Brightness Control	This is an OSC brightness control pin. The -Y output voltage when OSD is on can be adjusted using a DC voltage of 0 to 8V. When this pin is connected to V_{CC} with 100Ω, VCXO becomes a free-running oscillator and the horizontal and vertical blanking for the -Y output are disabled.	
37	Brightness Control	This is a -Y brightness control pin. The -Y output pedestal level can be adjusted between 2 to 7V for brightness control by using a DC voltage of 1 to 4V.	
38	Clamp. Filter	This is a clamp. filter terminal for the -Y signal DC restoration. The DC restoration rate correcting pulse added in the APL Det. circuit is DC-restored 100%.	
39	Contrast Control	This is a -Y contrast control /chroma uni-color control pin. The contrast and uni-color can respectively adjusted 20dB by using a DC voltage of 1 to 4V. This pin is pulled LOW, the vertical output pulse is disabled. This pin can be used for service mode when shipping from the factory.	
40	V/C/D V_{CC}	This is a V_{CC} pin for the video, chroma and deflection circuits.	—

PIN No.	PIN NAME	FUNCTION	INTERFACE CIRCUIT
41	Video Input	This is a video (-Y) signal input pin. Because a video trap and delay line are built-in here, you can do away with an external filter. The standard input signal is a 1.0V_{p-p} composite video signal.	
42	Sharpness Control	This is a sharpness control pin. The added pulse quantity can be adjusted from −5% to 15% by using a DC voltage of 1 to 4V. When this pin is pulled LOW, the vertical counter of the sync. count-down circuit is reset. Make sure this pin is pulled LOW when the TV set is switched on and channels are switched over.	
43	Chroma Input	This is a chroma signal input pin. This terminal contains a take-off filter for signal from PIF and a band-pass filter for external input. Selection between the two chroma filters is determined by the DC voltage on this pin. LOW level : Band-pass filter HIGH level : Take-off filter This pin has a 0.4V hysteresis to prevent the filters from being inadvertently switched over by the chroma signal. The standard chroma input is 280mV_{p-p}.	
44	APL Filter	This is an APL Det. filter terminal. The DC restoration rate is eased by adding a DC restoration rate correction pulse to the Y signal after detecting APL in video input signal and then restoring this pulse 100% in the final stage. The DC restoration rate can be adjusted by changing the filter constant.	

PIN No.	PIN NAME	FUNCTION	INTERFACE CIRCUIT
45	Black Level Det.	This is a black level Det. filter terminal. If detects the blacker-than-black level that determines the black-stretch gain. Its Det. sensitivity is determined by the value of an external resistor. The recommended value of the external CR time constant is approximately 0.1s. The black-stretch start point is 50 IRE. The peak black-stretch level is 15 IRE.	
46	PIF Output	This is a PIF Det. output pin. It generates a $2V_{p-p}$ Det. output for the standard PIF input. Although this is a split input type of PIF, make sure that this output is passed through and SIF trap before it is input to V/C/D, because the SIF component cannot always be completely removed depending on the SAW filters used. The minimum load resistance this output can drive is 2.7kΩ.	
47 51	RF AGC Delay RF AGC Output	These are RF AGC delay level adjustment pins. Use these pins to adjust the tuner's gain according to the field strength.	
48 49	VCO Tank 1 VCO Tank 2	Connect a PLL VCO tank coil for PIF Det. to this pin. Vary the capacitance of the built-in varicap to adjust the VCO oscillation frequency. The adjustment range is determined by the capacitance ratio with respect to the resonance capacitor. An approximate guide for this adjustment is such that a 30pF resonance capacitor provides a 2.3MHz wide adjustment range.	
50	2nd AGC	This is a PIF 2nd AGC filter terminal.	See pin 2.

PIN No.	PIN NAME	FUNCTION	INTERFACE CIRCUIT
52	AFT Tank	Connect an AFT tank coil to this pin. The AFT function can be muted by driving the voltage on this pin below 2.1V .	
53	SIF V_{CC}	This is a V_{CC} pin for the SIF demodulation circuit. It is recommended that a trap for the PIF carrier frequency be inserted in series to prevent characteristics degradation due to current leakage from V_{CC}. (In the applications circuit example a 68μH coil is inserted.) V_{CC} = 9V (Typ.)	—
54 55	FM Demodulation Input Limiter Output	These pins generate a 90° phase-shift signal for FM demodulation. The audio signal is muted by driving the voltage on pin 54 below 0.3V. The voltage on pin 56 at this time is about 4.5V. This terminal can be made adjustment-free by connecting a ceramic discriminator. However, adjustment is required for sound-multiplex demodulation, because the Det. bandwidth must be sufficiently large. For this adjustment, it is recommended that a tank coil and damping resistor be inserted in parallel.	
56	Audio Output	This is an audio output pin. When feeding this output to and external circuit, connect a 75μs de-emphasis circuit. The audio output is $1V_{p-p}$ (Typ.). The minimum load resistance this output can drive is 3.5kΩ.	

CONTROL SWITCH FUNCTION

PIN No.	CHARACTERISTIC	FUNCTION	CONDITION
2	EIA Decoder	Low : IF Amp. gain is fixed min.	0.2V
50	AFT Defeat	Low : AFT Defeat	2.1V
54	Audio Mute	Low : Sound Mute Pin 56 : 4.1V	0.3V
17	Chroma Output	High : Chroma signal can be Monitored at pin 17	Connected with V_{CC} by 2.2kΩ
36	VCXO Free-run	High : VCXO Free-run, H, V-Blanking on -Y output stop	8.3V
39	V Stop	Low : V. Pulse Stop	0.4V
42	V Counter Reset	Low : Internal V. Counter reset	0.5V
43	Chroma Filter Select	High : BPF Low : TOF selected	4.1V, 4.5V Shmittriger
9	f_{SC} Trap	Low : Chroma Trap is selected. High : Pass the Trap	0.3V

MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V_{CC}	12	V
Power Dissipation	P_{Dmax}	1.92 (Note)	W
Input Terminal Voltage	V_{in}	GND − 0.3~V_{CC} + 0.3	V
Input Signal Amplitude	e_{in}	4	V_{p-p}
Operating Temperature	T_{opr}	− 20~65	°C
Storage Temperature	T_{stg}	− 55~150	°C

(Note) When using the device at above Ta = 25°C, decrease the power dissipation by 15.3mW for each increase of 1°C.

RECOMMENDED CONDITION FOR OPERATING

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
PIF Supply Voltage	V_{CCP}	8.1	9.0	9.5	V	—
SIF Supply Voltage	V_{CCS}	8.1	9.0	9.5	V	—
V/C/D Supply Voltage	V_{CCV}	8.1	9.0	9.5	V	—
H.V_{CC} Supply Voltage	H.V_{CC}	6.5	6.8	7.1	V	—
Video Input Signal	V_{in41}	—	1.0	—	V_{p-p}	Involving Sync. Signal
Chroma Input Signal	V_{in43}	—	286	—	mV_{p-p}	Burst Signal Amp.
Sync. Input Signal	V_{in35}	1.0	2.0	—	V_{p-p}	—
DC Control Voltage	$V_{16, 17, 39}$ $V_{37, 42}$	1.0	—	4.0	V	TINT, Color, Contrast Brightness, Sharpness
	V_{36}	3.0	—	6.0	V	OSD Brightness
	V_{28}	GND	—	H.V_{CC}	V	H.Phase
FBP Width	T_{FBP}	10	12	—	μs	Pin 34 $V_{th} = 2V_F$
FBP Input Current	I_{FBPmax}	—	1.0	1.2	mA	—
Video Output Load Resistance	R_{OV}	2.7	7.5	—	kΩ	—
Sound Output Load Resistance	R_{OS}	2.6	8.2	—	kΩ	—
-Y Output Load Resistance	R_{O-Y}	3.5	10	—	kΩ	Observe these conditions during external blanking period.
Color Differential Load Resistance	R_{ORGB}	2.5	10	—		
H. Output Load Resistance	R_{HOUT}	0.5	0.8	—	kΩ	—
V. Output Load Resistance	R_{VOUT}	4.1	5.7	—	kΩ	—

ELECTRICAL CHARACTERISTICS (Unless otherwise specified, V_{CC} = 9V, H.V_{CC} = 6.8V, Ta = 25°C)
DC CHARACTERISTIC
Terminal voltage

CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
PIF Input 1	V_3	—	—	4.3	4.6	4.9	V
PIF Input 2	V_4	—	—	4.3	4.6	4.9	
SIF Input	V_6	—	—	3.0	3.3	3.6	
SIF Output	V_8	—	V_7 = 2.5V	2.7	3.0	3.3	
Limiter Input	V_9	—	—	—	4.6	—	
Loop Filter	V_{10}	—	V_{30} = 3V	3.8	4.1	4.4	
VCXO Input	V_{13}	—	—	2.8	3.1	3.4	
APC Filter	V_{14}	—	—	5.9	6.35	6.8	
VCXO Drive	V_{15}	—	—	5.9	6.25	6.6	
Tint Control	V_{16}	—	OPEN	—	5.0	—	
Color Control	V_{17}	—	OPEN, V_{36} = 9V	—	5.0	—	
R-Y Output	V_{23}	—	—	5.0	5.35	5.7	
B-Y Output	V_{24}	—	—	5.0	5.35	5.7	
G-Y Output	V_{25}	—	—	5.0	5.35	5.7	
32f_H VCO	V_{29}	—	—	3.4	3.7	4.0	
AFC Filter	V_{32}	—	—	2.1	2.35	2.6	
Video Input	V_{41}	—	—	3.6	3.9	4.2	
Chroma Input	V_{43}	—	OPEN	5.7	6.1	6.5	
APL Filter	V_{44}	—	OPEN	4.8	5.25	5.7	
Black Level Det.	V_{45}	—	—	5.5	5.9	6.3	
RF AGC Delay	V_{47}	—	OPEN	4.3	4.7	5.0	
FM Det. Input	V_{54}	—	—	3.15	3.45	3.75	

Supply current

CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
PIF Supply Current	I_{CCP}	—	V_{CC} = 9V	10	20	25	mA
SIF Supply Current	I_{CCS}	—	V_{CC} = 9V	10	20	25	
V/C/D Supply Current	I_{CCV}	—	V_{CC} = 9V	55	72	90	
H.V_{CC} Supply Current	H.I_{CC}	—	H.V_{CC} = 6.8V	13	15	25	

AC CHARACTERISTICS
PIF stage (PIF typical input level : 58.75MHz, 95dBμV)

CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
PIF Detected Output Level	V_{01}	—	PIF typical input level m = 87.5%AM	1.7	2.0	2.3	V_{p-p}
	V_{02}	—	PIF typical input level m = 110%AM	2.0	2.5	3.0	
PIF Sensitivity	$V_{IN\ MIN}$	—	f_m = 15.75kHz, m = 30%AM −3dB Point	39	43	47	dBμV
Max. PIF Input Level	$V_{IN\ MAX}$	—	f_m = 15.75kHz, m = 30%AM +0.5dB Point	94	100	—	dBμV
Sync. Tip Level	V_{SYNC}	—	PIF typical input level m = 87.5%AM	2.6	2.9	3.2	V
No Signal Level	V_{IF}	—	No input, V_{50} = 3V, Measure the V_{46}	4.8	5.2	5.6	V
DG	DG	—	PIF typical input level m = 87.5%AM	—	2	5	%
DP	DP	—	PIF typical input level m = 87.5%AM	—	2	5	°
PIF Output Frequency Characteristic	f_c	—	(Note 1)	5	7	10	MHz
Suppression Carrier	CR	—	(Note 2)	45	50	—	dB
Suppression 2nd Harmonic Carrier	HR			45	50	—	
Black Noise Inverter Level	V_{BTH}	—	(Note 3)	1.9	2.1	2.4	V
Black Noise Clamp Level	V_{BCL}			3.4	3.7	4.0	
White Noise Inverter Level	V_{WTH}	—	(Note 4)	5.5	5.8	6.1	V
White Noise Clamp Level	V_{WCL}			3.4	3.7	4.0	
PIF Input Impedance	R_{iPIF}	—	V_{50} = 3V	—	1.5	—	kΩ
PIF Input Capacitance	C_{iPIF}	—	V_{50} = 3V	—	3.8	—	pF
S / N	S / N	—	(Note 5)	52	55	—	dB
920kHz Beat	I_{920}	—	(Note 6)	38	45	—	dB
IF AGC Range	RW_{AGC}	—	$RW_{AGC} = V_{IN\ MAX} - V_{IN\ MIN}$	54	57	60	dBμV

CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
IF AGC Voltage	V_{50MRAN}	—	PIF Input : 58.75MHz CW Measure the voltage of pin 50. Input Level 84dBμV : V_{50MEAN} 110dBμV : V_{50MIN} No Input : V_{50MAX}	5.3	5.6	5.9	V
	V_{50MAX}			8.3	8.5	—	
	V_{50MIN}			—	3.0	—	
RF AGC Output	V_{51MAX}	—	Adjustment VR_{47} to maintain V_{51} = 4.5V. Input Level V_{51MAX} : No input V_{51MIN} : 110dBμV	8.5	9.0	—	V
	V_{51MIN}			—	0	0.5	
RF AGC Gain	$G_{RF\ AGC}$	—	$G_{RF\ AGC} = 20\ell og \frac{\Delta V_{51}}{\Delta V_{50}}$	38	41	44	dB
AFT Center Voltage	V11CRNT	—	No input, V_{50} = 3V, Measure the voltage of V_{11}	3.0	4.5	6.0	V
AFT Mute-offset Voltage	V_{11OFFS}	—	(Note 7)	−2.0	0	2.0	V
AFT Voltage	V_{11MAX}	—	f_m = 15.75kHz, m = 30%AM Measure the voltage of pin 11.	8.3	8.6	—	V
	V_{11MIN}			—	0.3	0.7	
AFT Sensitivity	μ_{AFT}	—	Center : f = 58.75MHz	—	20	25	kHz / V
VCO Control Sensitivity	β_{IFVCO}	—	—	1.0	1.5	—	MHz / V
VCO Pull-in Range	f_{ph}	—	Center : f = 58.75MHz	0.5	0.7	—	MHz
	f_{pl}		Center : f = 58.75MHz	0.5	1.0	—	

SIF stage (Typical SIF input level : f = 4.5MHz, f_m = 400Hz, FM 25kHz / devi, 100dBμV)

CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
1st SIF Output Level	V_{S1}	—	PIF input 58.75MHz, 75dBμV SIF input 54.25MHz, 75dBμV V_{S1} : 4.5MHz level of SIF output	90	100	110	dBμV
SIF AGC Voltage	$V_{1\ AGC}$		$V_{1\ AGC}$: Pin 1 voltage in this condition	3.2	3.5	3.8	V
1st SIF Gain	$G_{S\ MAX}$	—	Note 8	9	13	17	dB
	$G_{S\ MIN}$			− 11	− 15	− 19	
1st SIF Input Impedance	R_{iSIF}	—	—	—	1	—	kΩ
1st SIF Input Capacitance	C_{iSIF}	—	—	—	2	—	pF
Audio Output Level	V_{AAC}	—	Limiter input : 4.5MHz, fm = 400Hz FM 25kHz / devi, 100dBμV 75μs De-emphasis output	350	450	600	mV_{rms}
	V_{ADC}			4.2	4.5	4.8	V
AD Distortion	K_{AUDIO}	—	Limiter input : 4.5MHz, fm = 400Hz FM 25kHz / devi, 100dBμV 75μs De-emphasis output distortion	—	0.3	1.0	%
AMR	AMR	—	FM OFF 30% AM V_{56AC} / V_{AAC}	48	58	—	dB
Limiting Sensitivity	V_{LIM}	—	Input Level − 3dB point	—	35	45	dBμV
AF Bandwidth	f_{AUDIOH}	—	Input frequency − 3dB point	70	110	—	kHz
	f_{AUDIOL}			− 70	− 110	—	

Video stage

CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Input Impedance	R_{i41}	—	—	100	—	—	kΩ
Input Dynamic Range	V_{di41}	—	Concerning video signal	0.9	1.0	1.2	V
Video Gain	G-Y	—	Contrast : Max. Black Expander : OFF	4.7	5.5	6.0	
Video Frequency Characteristic	f-Y	—	– 3dB Point	7.0	8.0	—	MHz
Output Min. Voltage	V_{do1}	—	Input $1V_{p-p}$ Brightness and contrast : Max.	—	1.2	1.5	V
Black Peak Level	R_{BOUT}	—	(Note 9)	2	5	8	IRE
Black Expander Start Point	R_{BSTP}			40	55	68	
DC Restoration Ratio	T_{DC}	—	(Note 10)	98	103	106	%
Sharpness Control Characteristics	G_{SHcent}	—	V_{42} = 1.5V Sharpness shoot ratio	– 5	0	5	%
	G_{SHmax}		V_{42} = 4V Sharpness shoot ratio	25	40	55	
	G_{SHmin}		V_{42} = 1V Sharpness shoot ratio	– 15	– 12	– 8	
Sharpness Delay Time	t_{SHDLY}	—	Sharpness shoot width	—	160	—	ns
Contrast Control Characteristics	ΔG_{CNT}	—	Y total gain variable range	18	20	—	dB
Brightness Control Characteristics	V_{BRTCEN}	—	V_{37} = 2.5V Pedestal level of – Y output	4.4	4.7	5.0	V
	ΔV_{BRT}	—	Brightness variable range	± 2.5	± 2.8	—	
H, V-BLK Output Level	V_{BLK}	—	—	8.5	8.9	9.0	V
V-BLK Width	T_{VBLK}	—	—	—	16	—	H
Chroma Trap Gain	G_{trap}	—	—	—	– 18	– 15	dB

OSD stage

CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
OSD Switching Threshold	V_{thOSD}	—	R, G, B fast blacking	0.7	1.0	1.3	V
OSD Delay Time	t_{OSDDLY}	—	OSD brightness control : center -Y output width	—	15	40	ns
OSD Delay Time Tracking	Δt_{OSDD}	—		—	15	30	ns
OSD Rising Time	τ_R	—		—	15	40	ns
OSD Falling Time	τ_F	—		—	18	40	ns
OSD Color Difference Output Level	V_{OSDDIF}	—	OSD color difference output level	6.4	6.7	7.0	V
	V_{OSDCLP}		Output clamp level of other colors.	4.0	4.3	4.6	
OSD Brightness Control Characteristics	V_{OSDCEN}	—	V_{36} = 4.5V OSD-Y output level	3.2	3.9	4.6	V
	ΔV_{OSDY}		OSD-Y output variable range	6.0	6.5	7.0	

Chroma stage (Typical chroma input level 0dB : 286mV$_{p-p}$, f_{SC} = 3.579545MHz)

CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Input Impedance	R_{i43}	—	SW43 : OPEN	—	3.0	—	kΩ
Input Dynamic Range	V_{di43}	—	Include sync. and video signal	1.0	1.5	1.7	V
ACC Characteristics	ea	—	(Note 11)	−23	−20	−17	dB
	eb			3	6	9	
	A			0.9	1.00	1.1	
Color Killer Point	E_K	—	Killer OFF→ON	−46	−43	−37	dB
Color Control Characteristics	V_{CLRCEN}	—	Pin 17 voltage at which color gain is center.	2.2	2.5	2.8	V
	ΔG_{CLR}	—	Color gain variable range	40	43	—	dB
Uni-color Control Characteristics	V_{UNICEN}	—	Pin 39 voltage at which Uni-color gain is center	2.2	2.5	2.8	V
	ΔG_{UNI}	—	Chroma Uni-color variable range	18	20	—	dB
TINT Control Characteristics	V_{TNTCEN}	—	(Note 12)	2.2	2.5	2.8	V
	$\Delta\theta_{TINT}$	—	Tint variable range	75	85	100	°
VCXO Control Range	Δf_{VCXO}	—	—	±500	±650	—	Hz
VCXO Control Sensitivity	β_{VCXO}	—	—	—	1.0	—	Hz / mV
VCXO Pull-in Range	f_{VCXOPL}	—	—	±400	±550	±750	Hz
	V_{DM}	—	—	4.8	5.4	6.0	V
Color Difference Output DC Level	ΔV_{DM}	—	—	—	±0.1	±0.3	V
Color Difference Output Amplitude	E_{Bmax}	—	(B-Y) Maximum amplitude	4.2	4.5	—	V_{p-p}
Relative Amplitude	R / B	—	(R-Y) / (B-Y)	0.80	0.84	0.90	
	G / B		(G-Y) / (B-Y)	0.25	0.28	0.31	
Relative Phase	R-B	—	—	97	105	113	°
	G-B		—	241	249	257	
Color Differential Output Residual Levels	E_{CR}	—	Color, Uni-Color : Center	—	20	30	mV_{p-p}
	E_{CB}			—	20	30	
	E_{CG}			—	20	30	
Video-chroma Delay Time	t_{V-C}	—	(Video delay time) − (Chroma delay time)	—	40	75	ns

Deflection stage

CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Horizontal Oscillation	f_H	—	(Free run frequency) – (15.734kHz)	– 100	100	300	Hz
H. Output pulse Duty	T_H	—	—	35	37	40	%
H. Output Level	V_{HL}	—	H. Output low level voltage	—	0.2	0.3	V
	V_{HH}	—	H. Output high level voltage	4.2	4.6	—	
H. VCO Start Voltage	V_{OSCmin}	—	H.V_{CC} voltage at which $32f_H$ VCO starts to oscillate	3.4	3.6	4.0	V
H. Output Start Voltage	V_{HST}	—	H.V_{CC}	4.1	4.3	4.5	V
H. Frequency Control Range	Δf_H	—	Center : f_H = 15.734kHz	± 500	± 650	—	Hz
H. VCO Control Sensitivity	β_H	—	—	—	350	—	Hz / V
H. AFC Pull-in Range	Δf_{HPUL}	—	Center : f_H = 15.734kHz	± 450	± 500	—	Hz
X-ray Protect Detection Voltage	V_{XDET}	—	(Note 13)	3.2	3.5	3.8	V
X-ray Protect Holding Voltage	V_{XHLD}			3.9	4.2	4.5	
X-ray Protect Holding Current	I_{XHLD}			80	100	120	μA
Vertical Frequency	f_V	—	Free run frequency	—	262.5	—	H
V. OSC Pull-in Range	T_{VST}	—	V. Pull-in starting time	—	+ 32	—	H
	T_{VEND}		V. Pull-in stopping time	—	– 32	—	
V. OSC Pulse Width	T_V	—	—	—	10	—	H
V. Output Pulse Level	V_{VL}	—	V. Output low level voltage	—	0.2	0.3	V
	V_{VH}		V. Output High level voltage	4.8	5.3	—	
H. Sync. Sepa. Level	R_{sepa}	—	(Note 14)	10	16	25	%

TEST CONDITION

(Note 1) PIF output frequency characteristic

(1) PIF input $f = 58.75MHz$, $84dB\mu V$, CW

(2) Fix the voltage of 2nd AGC on this condition

(3) PIF input $f_0 = 58.75MHz$, $84dB\mu V$
$f_1 = 58.65 \sim 45MHz$, $74dB\mu V$

(4) Measure f_1 at which PIF output turns to $-3dB$

(5) $f_c = f_0 - f_1$

(Note 2) Suppression carrier, suppression 2nd harmonic Carrier

(1) PIF input $f = 58.75MHz$, $f_m = 15.75kHz$, $84dB\mu V$, 78%AM

(2) Apply external voltage to get 2Vp-p PIF output

(3) Measure the carrier leakage in PIF output with spectrum analyzer. (no modulation)

(4)

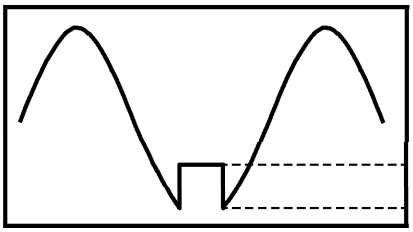
$$CR = 20\ell og \frac{2\,(V_{p\text{-}p})}{\text{Carrier leak } (mV_{rms})} \quad [dB]$$

(5) Measure the suppression 2nd harmonic carrier in same way.

(Note 3) Black noise inverter level, black noise clamp level

(1) PIF input $f = 58.75MHz$, $f_m = 15.75kHz$, $84dB\mu V$, 30%AM

(2) Raise the 2nd AGC voltage up to a level to get following wave form, and measure A, B voltage.

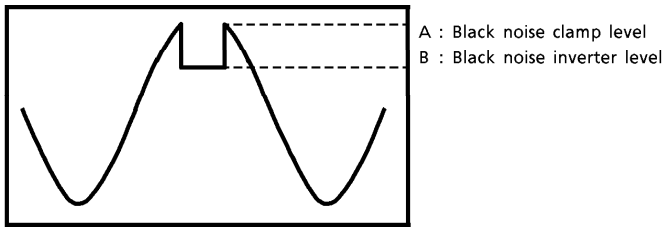


PIF output wave form

(Note 4) White noise inverter level, White noise clamp level

(1) PIF input f = 58.75MHz, 95dBμV, CW

(2) Detune the VCO tank, monitor the PIF output and measure A, B voltage.



PIF output wave form

(Note 5) S / N

(1) PIF input f = 58.75MHz, 95dBμV
A : f_m = 15.75kHz, 30% AM
B : CW

(2) Measure the voltage of PIF output

(3)

$$SN = 20\ell og\left(\frac{V_A}{V_B} \times 6\right) \quad [dB]$$

(Note 6) 920kHz beat

(1) PIF input f_0 = 58.75MHz, 84dBμV
f_C = 55.17MHz, 74dBμV
f_S = 54.25MHz, 74dBμV
input with Mix. pad.

(2) Apply external voltage to get same level PIF output low level and V_{SYNC}.

(3) Measure the ratio of "f_C components VS 920kHz beat components" with spectrum analyzer.

(Note 7) AFT Mute-offset voltage

(1) PIF input No input, V_{50} = 3V

(2) Measure V_{11} at AFT mute SW on : V_{11MUTE}

(3) $V_{11OFFS} = V_{11CENT} - V_{11MUTE}$

(Note 8) 1st SIF gain

(1) PIF input $f_0 = 58.75MHz$, $75dB\mu V$
SIF input $f_S = 54.25MHz$, $75dB\mu V$

(2) Measure the level of the 4.5MHz component from the 1st SIF output pin. V_8

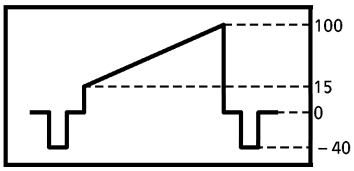
(3) When the SIF input level is varied under the following conditions, relative to V8
Input level difference at $-3\,dB$: $G_{S\ MAX}$ However, $V_1 = 4.5V$
Input level difference at $+3dB$: $G_{S\ MIN}$ However, $V_1 = 3.0V$

(Note 9) Black peak level and black expander start point

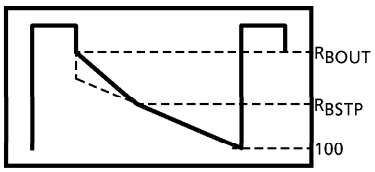
(1) Input the $1V_{p-p}$ video signal shown below to the video input.

(2) Disable the black-stretch function by setting $V_{45} = 5V$

(3) Measure the blacker-than-black blanking level R_{BOUT} at the -Y output and the black-stretch start level.



Input signal : Blacker-than-black blanking level 15 IRE



-Y output

(Note 10) DC restoration

(1) Disable the black-stretch function by setting $V_{45} = 5V$. With pin 44 left open.

(2) Vary the video input APL 10~90%.

(3) Adjust the video signal amp. litude at the -Y output to become 1.25V.

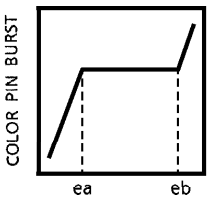
(4) Assuming that the pedestal level change due to APL changes is ΔV_{pede}, then
$T_{CD} = (1V - \Delta V_{pede}) \times 100\,[\%]$

(Note 11) ACC characteristic

(1) Connect the color control pin to V_{CC} with $2.2\,k\Omega$.

(2) $V_{39} = 1V$

(3) While varying the burst level of the chroma input, measure the burst level appearing at the color pin.



INPUT SIGNAL BURST LEVEL
$0dB = 286mV_{p-p}$

(4)

$$A = \frac{V_{B\ (3dB)}}{V_{B\ (-17dB)}}$$

(Note 12) Tint control characteristics

(1) Input the rainbow color bar.

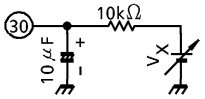
(2) Adjust the voltage of V_{16} until the No.6 color bar becomes maximum at the (B-Y) output.

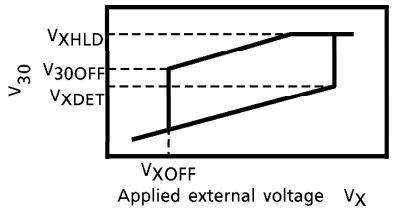
(Note 13) X-ray protect detection voltage, X-ray protect holding voltage, X-ray protect holding current.

(1) While varying external voltage source VX, measure V_{XDET} and V_{XHLD}.

(2) Measure V_{30OFF}, V_{XOFF}

$$I_{XHLD} = \frac{V_{30OFF} - V_{XOFF}}{10k\Omega}$$

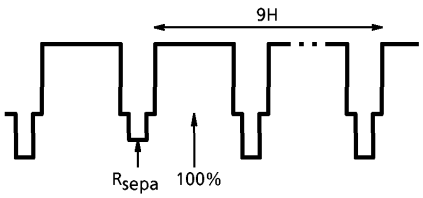




(Note 14) H. Sync. sepa. level

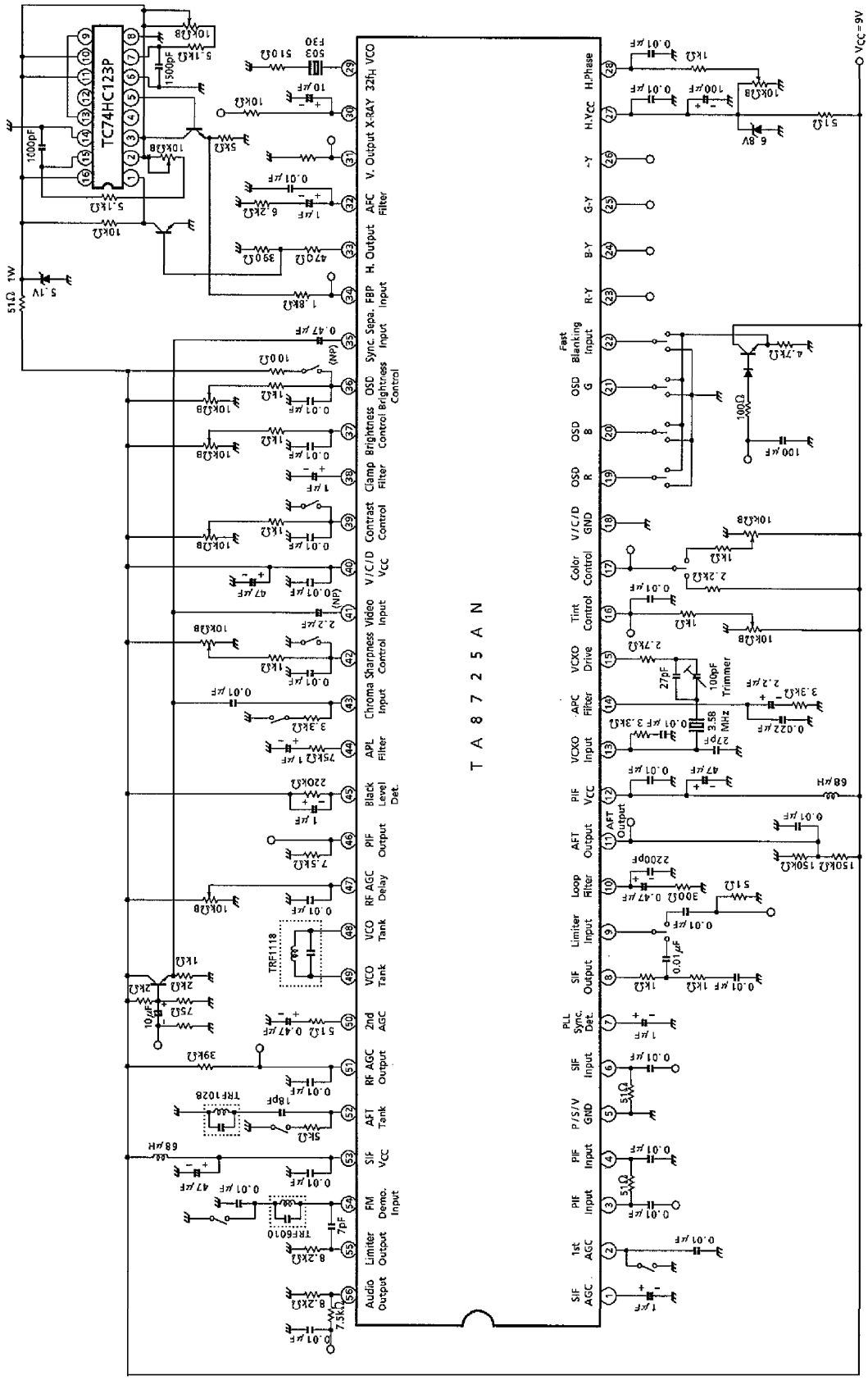
(1) Input a white-100 % signal (Where the sync. signal level is small every 10H) to the sync. separation pin.

(2) While observing the sync. signal appearing at the FBP input pin, measure the R_{sepa} level at which the sync. signal does no longer appear.



Sync. separation input

TEST CIRCUIT



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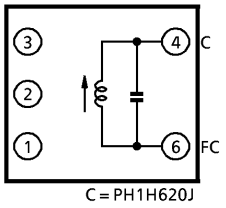
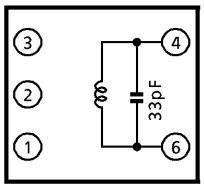
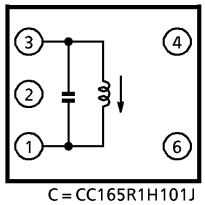
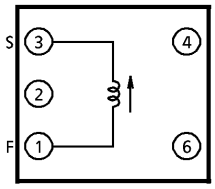
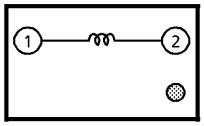
ADJUSTING MEASUREMENT CIRCUIT

1. PIF VCO tank coil
   (1) Make sure that nothing is fed to the PIF input, then fix the 2nd AGC pin to 3V.
   (2) Measure the voltage on the loop filter pin. V_A
   (3) Release the voltage on the 2nd AGC pin fixed to 3V.
   (4) PIF input f = 58.75MHz, 84dBμV
   (5) Adjusting the VCO tank coil until the voltage on the loop filter pin equals V_A.
2. AFT tank coil
   (1) Make sure that noting is fed to the PIF input, then fix the 2nd AGC pin to 3V.
   (2) Measure the voltage on the AFT output pin. V_{11CENT}
   (3) Release the voltage on the 2nd AGC pin fixed to 3V.
   (4) PIF input f = 58.75MHz, f_m = 15.75kHz, 84dBμV, 30%AM
   (5) Adjust the AFT tank coil until the voltage on the AFT output pin equals V_{11CENT}.
3. FM demodulation coil
   (1) Make sure that noting is fed to the limiter input.
   (2) Measure the voltage on the audio output pin. V_{ADC}
   (3) Limiter input f = 4.5MHz, 100dBμV, non-modulated
   (4) Adjust the AFT tank coil until the voltage on the audio output pin equals V_{ADC}.
4. VCXO oscillation frequency
   (1) Make sure that noting is fed to the chroma input, and connect the OSD brightness control pin to V_{CC} with 100Ω.
   (2) Measure the voltage on the APC filter terminal. V_{APC}
   (3) Chroma input f = 3.579545MHz, 280mV_{p-p}, CW
   (4) Adjust the trimmer capacitor at the VCXO drive terminal until the voltage on the APC filter terminal equals V_{APC}.

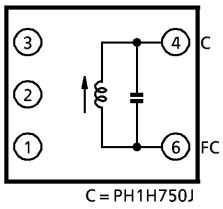
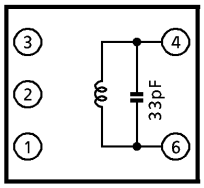
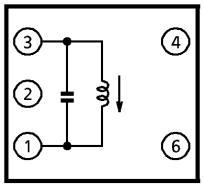
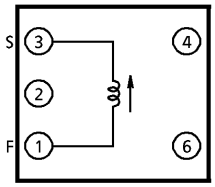
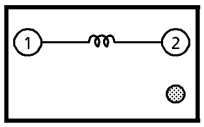
PRECAUTIONS TO BE TAKEN WHEN MEASURING ELECTRICAL CHARACTERISTICS

1. When measuring the PIF VCO oscillation frequency, measure the leakage component from the PIF output pin with spectrum analyzer.
2. When measuring the VCXO oscillation frequency, measure the leakage component from the color difference output pin with a spectrum analyzer.

DETAILS OF TANK COILS USED

TANK NAME	PRODUCT NAME	CONNECTION DIAGRAM	ELECTRICAL CHARACTERISTICS	
AFT Coil	TRF-1028	 C = PH1H620J	f_0 MAX	71.0MHz −8% or more (Auxiliary coil 30~100MHz)
			f_0 MIN	55.0MHz +8% or more (Auxiliary coil 30~100MHz)
			Non-load Q	Within 48 ± 25% (f_0 MIN)
VCO Tank	TRF-1118K		f_0 variable range	64MHz ± 3% (actual 58~70MHz)
			Non-load Q	110 ± 30%
SIF Tank	TRF-6010	 C = CC165R1H101J	Center frequency	4.5MHz (nominal)
			Demodulation output	77mV ± 10mV
			Tuning frequency	4.467MHz ± 11kHz
SAW-P Coil	TRF-1058		Fixed L	0.52μH ± 10% (f = 25.5MHz)
			Non-load Q	Within 50 ± 20% (f = 25.5MHz)
SAW-S Coil	TRF-1090		Fixed L	0.65μH ± 10%
			Non-load Q	85 ± 15% (f = 25.2MHz)
			Temperature coefficient	0 ± 60ppm

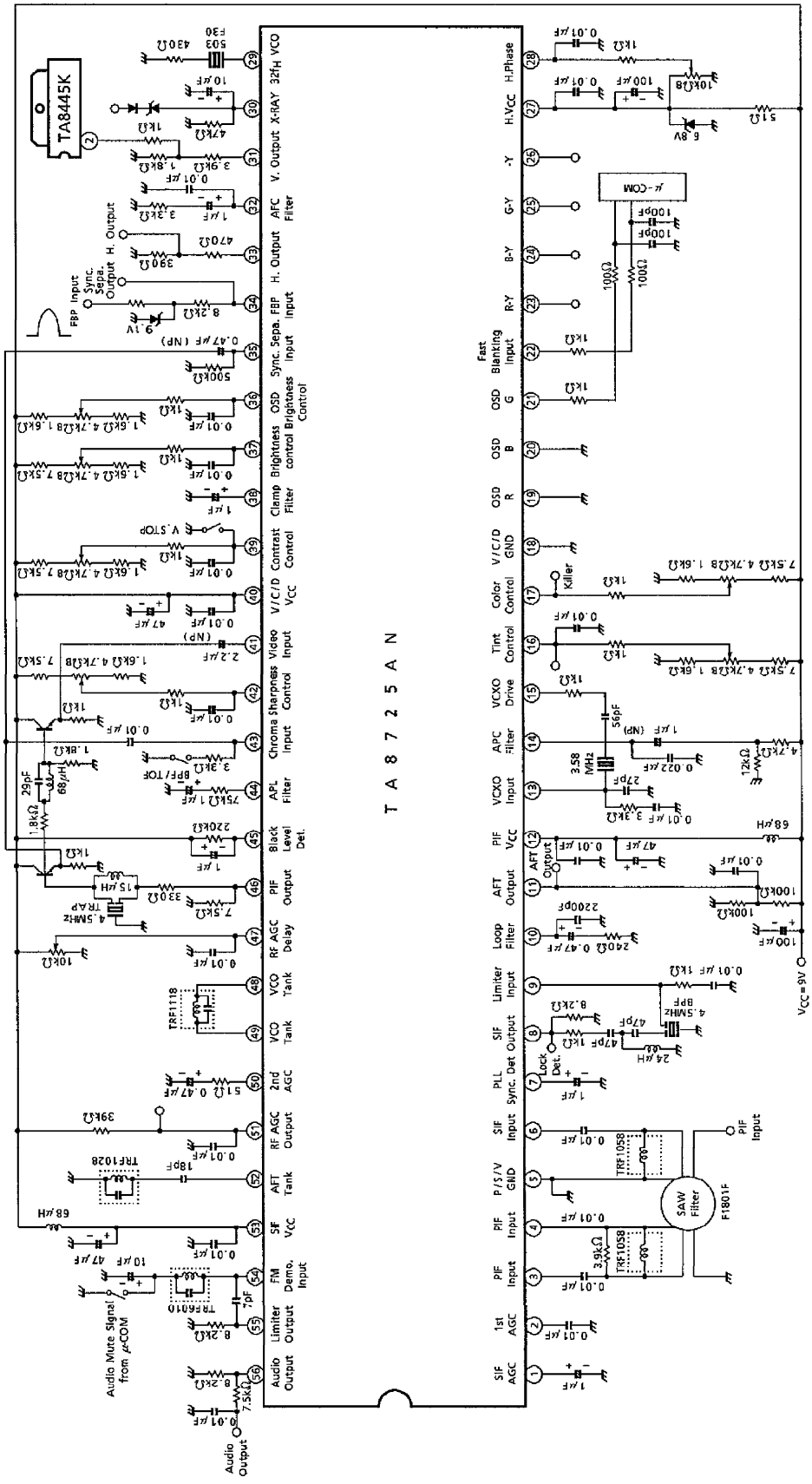
TA8725AN (for use in Japan)

TANK NAME	PRODUCT NAME	CONNECTION DIAGRAM	ELECTRICAL CHARACTERISTICS	
AFT Coil	TRF-1223	 C = PH1H750J	f_0 MAX	55.5MHz −8% 以上 (Auxiliary coil 30~100MHz)
			f_0 MIN	42.8MHz +8% 以上 (Auxiliary coil 30~100MHz)
			Non-load Q	Within 65 ± 25% (f_0 MIN)
VCO Coil	TRF-1130D		f_0 variable range	53.0MHz ± 3% (actual 50~70MHz)
			Non-load Q	128 ± 30%
SIF Tank	TRF-6010	 C = CC165R1H101J	Center frequency	4.5MHz (nominal)
			Demodulation output	77mV ± 10mV
			Tuning frequency	4.467MHz ± 11kHz
SAW-P Coil	TRF-1058		Fixed L	0.52μH ± 10% (f = 25.5MHz)
			Non-load Q	Within 50 ± 20% (f = 25.5MHz)
SAW-S Coil	TRF-1090		Fixed L	0.65μH ± 10%
			Non-load Q	85 ± 15% (f = 25.2MHz)
			Temperature coefficient	0 ± 60ppm

TA8725AN (For use in U. S.)

APPLICATION CIRCUIT

(For Japan)



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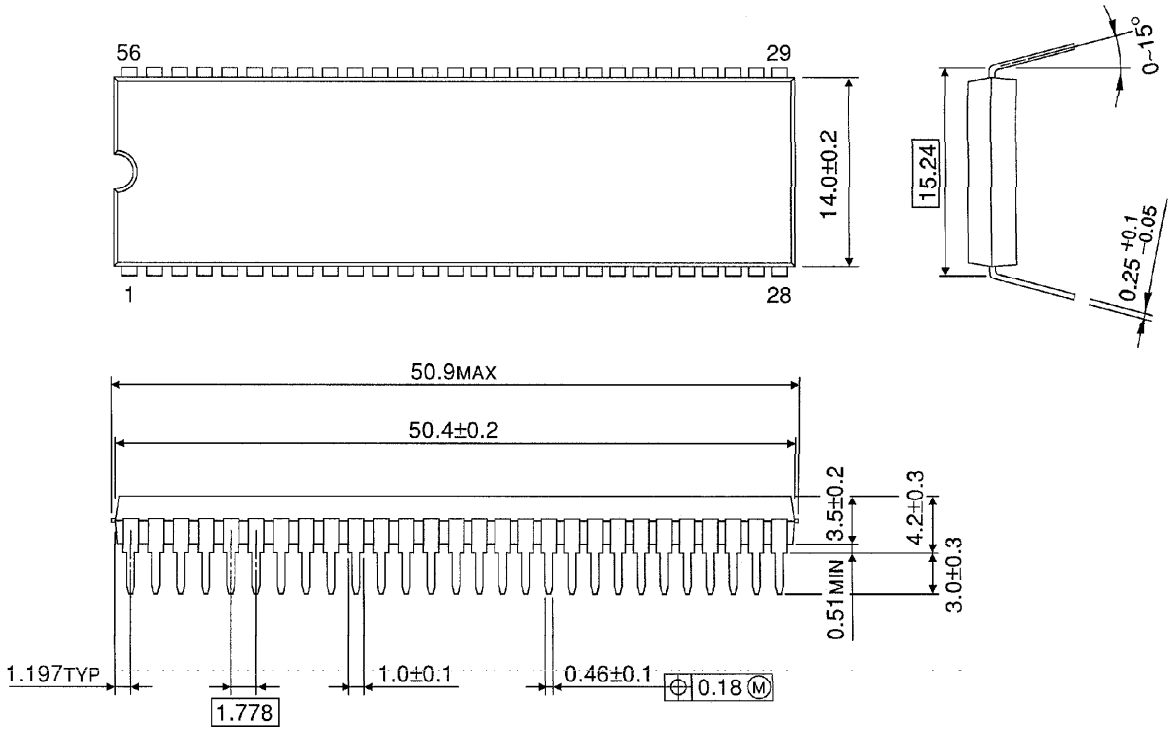
PACKAGE DIMENSIONS

SDIP56-P-600-1.78 Unit : mm



Weight : 5.55g (Typ.)

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