MOTOROLA

MC44818

PLL Tuning Circuit with I2C Bus

The MC44818 is a tuning circuit for TV and VCR tuner applications. It contains, on one chip, all the functions required for PLL control of a VCO. This integrated circuit also contains a high frequency prescaler and thus can handle frequencies up to 1.3 GHz. The MC44818 is a pin compatible drop in replacement for the MC44817, where the only difference is the MC44818 has a fixed divide–by–8 prescaler (cannot be bypassed) and the MC44817 uses the three wire bus.
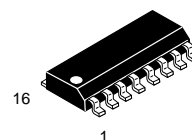
The MC44818 has a programmable 512/1024 reference divider and is manufactured on a single silicon chip using Motorola's high density bipolar process, MOSAIC™ (Motorola Oxide Self Aligned Implanted Circuits).

- Complete Single Chip System for MPU Control (I2C Bus). Data and Clock Inputs are 3–Wire Bus Compatible
- Divide–by–8 Prescaler Accepts Frequencies up to 1.3 GHz
- 15 Bit Programmable Divider Accepts Input Frequencies up to 165 MHz
- Reference Divider: Programmable for Division Ratios 512 and 1024.
- 3–State Phase/Frequency Comparator
- Operational Amplifier for Direct Tuning Voltage Output (30 V)
- Four Integrated PNP Band Buffers for 40 mA (V_{CC1} to 14.4 V)
- Output Options for the Reference Frequency and the Programmable Divider
- High Sensitivity Preamplifier
- Circuit to Detect Phase Lock
- Fully ESD Protected

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TV AND VCR PLL TUNING CIRCUIT WITH 1.3 GHz PRESCALER AND I2C BUS
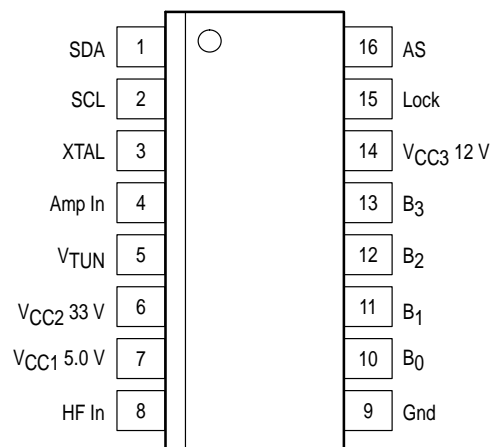
SEMICONDUCTOR TECHNICAL DATA

D SUFFIX
PLASTIC PACKAGE
CASE 751B
(SO–16)

PIN CONNECTIONS

SDA	1	16	AS
SCL	2	15	Lock
XTAL	3	14	V_{CC3} 12 V
Amp In	4	13	B_3
V_{TUN}	5	12	B_2
V_{CC2} 33 V	6	11	B_1
V_{CC1} 5.0 V	7	10	B_0
HF In	8	9	Gnd

(Top View)

ORDERING INFORMATION

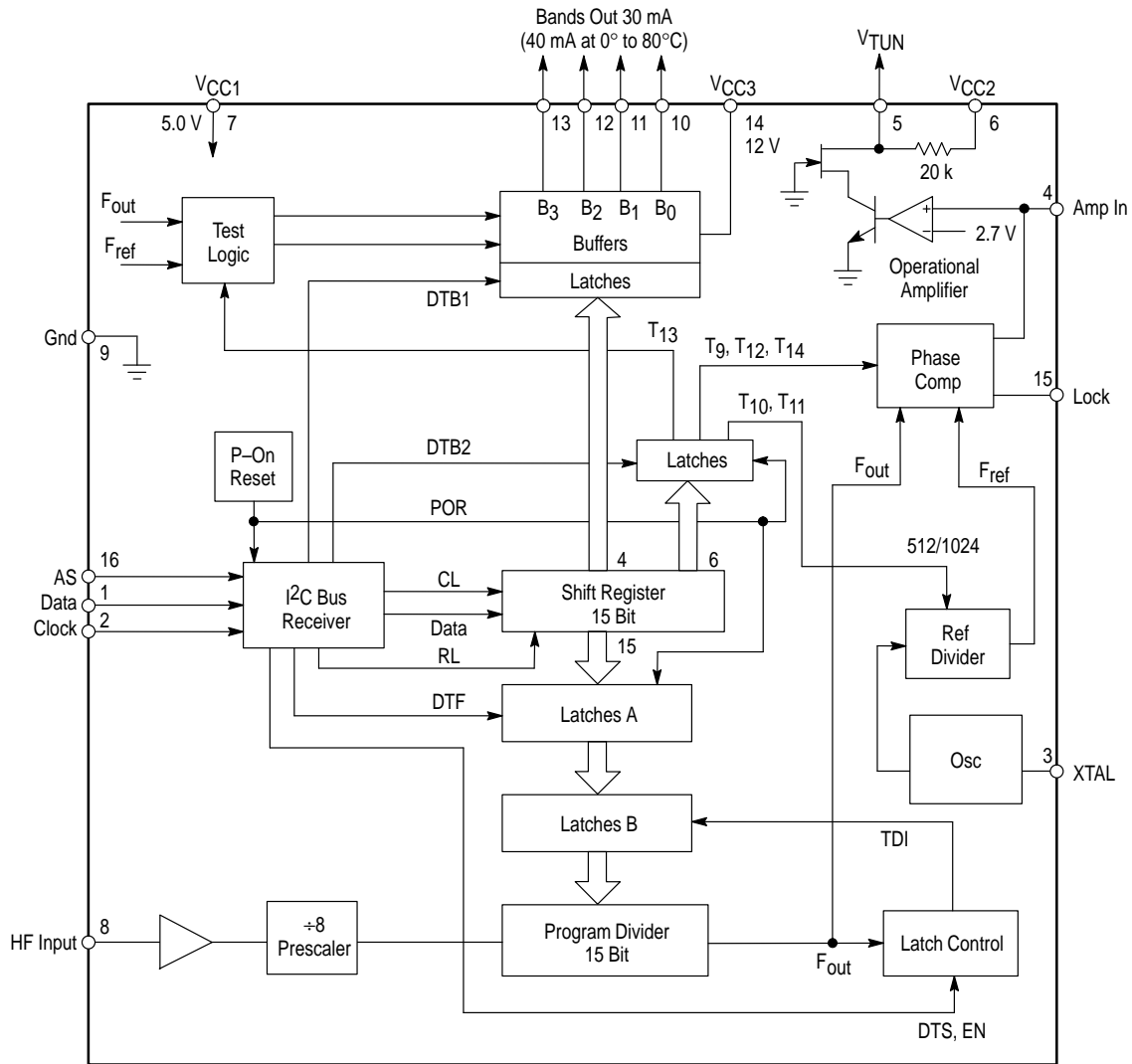| Device	Operating Temperature Range	Package
MC44818D	$T_A = -20°$ to $+80°C$	SO–16

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Representative Block Diagram

This device contains 3,204 active transistors.

MAXIMUM RATINGS (T_A = 25°C, unless otherwise noted.)

Rating	Pin	Value	Unit
Power Supply Voltage (V_{CC1})	7	6.0	V
Band Buffer "Off" Voltage	10–13	14.4	V
Band Buffer "On" Current	10–13	50	mA
Band Buffer – Short Circuit Duration (0 to V_{CC3}) (Note 2)	10–13	Continuous	–
Operational Amplifier Power Supply Voltage (V_{CC2})	6	40	V
Operational Amplifier Short Circuit Duration (0 to V_{CC2})	5	Continuous	–
Power Supply Voltage (V_{CC3})	14	14.4	V
Storage Temperature	–	−65 to +150	°C
Operating Temperature Range	–	−20 to +80	°C
Band Buffer Operation (Note 1) at 50 mA each Buffer All Buffers "On" Simultaneously	10–13	10	sec
Operational Amplifier Output Voltage	5	V_{CC2}	V
RF Input Level (10 MHz to 1.3 GHz)	–	1.5	Vrms

NOTES: 1. At V_{CC3} = V_{CC1} to 14.4 V and T_A = −20° to +80°C.
2. At V_{CC3} = V_{CC1} to 14.4 V and T_A = −20° to +80°C one buffer "On" only.

MC44818

ELECTRICAL CHARACTERISTICS (V_{CC1} = 5.0 V, V_{CC2} = 33 V, V_{CC3} = 12 V, T_A = 25°C, unless otherwise noted.)

| Characteristic	Pin	Min	Typ	Max	Unit
V_{CC1} Supply Voltage Range	7	4.5	5.0	5.5	V
V_{CC1} Supply Current (V_{CC1} = 5.0 V)	7	–	37	50	mA
V_{CC2} Supply Voltage Range	6	25	–	37	V
V_{CC2} Supply Current (Output Open)	6	–	1.5	2.3	mA
Band Buffer Leakage Current when "Off" at 12 V	10–13	–	0.01	1.0	µA
Band Buffer Saturation Voltage when "On" at 30 mA	10–13	–	0.15	0.3	V
Band Buffer Saturation Voltage when "On" at 40 mA only for 0° to 80°C	10–13	–	0.2	0.5	V
Data/Clock Current at 0 V	1, 2	–10	–	0	µA
Clock Current at 5.0 V	2	0	–	1.0	µA
Data Current at 5.0 V Acknowledge "Off"	1	0	–	1.0	µA
Data Saturation Voltage at 15 mA Acknowledge "On"	1	–	–	1.0	V
Data/Clock Input Voltage Low	1, 2	–	–	1.5	V
Data/Clock Input Voltage High	1, 2	3.0	–	–	V
Clock Frequency Range	2	–	–	100	kHz
Oscillator Frequency Range	3	3.15	3.2	4.05	MHz
Operational Amplifier Internal Reference Voltage	–	2.0	2.75	3.2	V
Operational Amplifier Input Current	4	–15	0	15	nA
DC Open Loop Voltage Gain	–	100	250	–	V/V
Gain Bandwidth Product (C_L = 1.0 nF)	–	0.3	–	–	MHz
V_{out} Low, Sinking 50 µA	5	–	0.2	0.4	V
V_{out} High, Sourcing 10 µA, $V_{CC2} - V_{out}$	5	–	0.2	0.5	V
Phase Detector Current in the High Impedance State	4	–15	0	15	nA
Charge Pump High Current of Phase Comparator	4	30	50	85	µA
Charge Pump Low Current of Phase Comparator	4	10	15	30	µA
V_{CC3} Supply Voltage Range	14	V_{CC1}	–	14.4	V
V_{CC3} Supply Current All Buffers "Off" One Buffer "On" when Open One Buffer "On" at 40 mA	14	– – –	0.2 8.0 48	0.5 13 53	mA

Data Format and Bus Receiver

The circuit receives the information for tuning and control via the I^2C bus. The incoming information, consisting of a chip address byte followed by two or four data bytes, is treated in the I^2C bus receiver. The definition of the permissible bus protocol is shown below:

1_STA CA CO BA STO
2_STA CA FM FL STO
3_STA CA CO BA FM FL STO
4_STA CA FM FL CO BA STO

STA = Start Condition
STO = Stop Condition
CA = Chip Address Byte
CO = Data Byte for Control Information
BA = Band Information
FM = Data Byte for Frequency Information
FL = Data Byte for Frequency Information

Figure 1. Complete Data Transfer Process
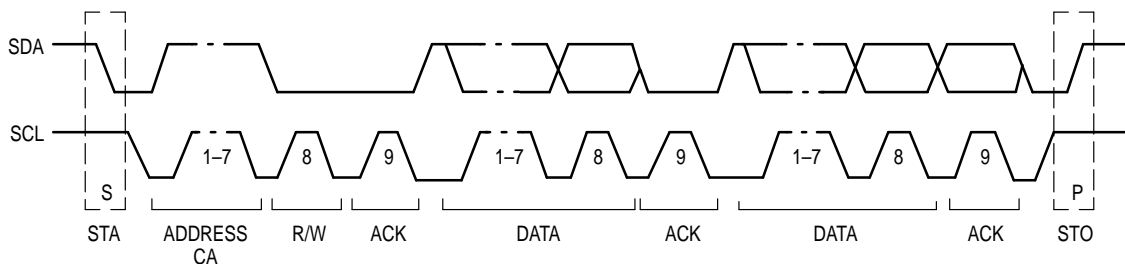
Figure 2 shows the five bytes of information that are needed for circuit operation: there is the chip address, two bytes of control and band information and two bytes of frequency information.

After the chip address, two or four data bytes may be received: if three data bytes are received the third data byte is ignored.

If five or more data bytes are received the fifth and following data bytes are ignored and the last acknowledge pulse is sent at the end of the fourth data byte.

The first and the third data bytes contain a function bit which allows the IC to distinguish between frequency information and control plus band information.

Frequency information is preceded by a Logic "0". If the function bit is Logic "1" the two following bytes contain control and band information. The first data byte, shifted after the chip address, may be byte CO or byte FM.

The two permissible bus protocols with five bytes are shown in Figure 2.

Figure 2. Definition of Bytes

CA_Chip Address	1	1	0	0	0	0/1	0/1	0	ACK
CO_Information	①	T_{14}	T_{13}	T_{12}	T_{11}	T_{10}	T_9	T_8	ACK
BA_Band Information	X	X	X	X	B_3	B_2	B_1	B_0	ACK
FM_Frequency Information	⓪	N_{14}	N_{13}	N_{12}	N_{11}	N_{10}	N_9	N_8	ACK
FL_Frequency Information	N_7	N_6	N_5	N_4	N_3	N_2	N_1	N_0	ACK

CA_Chip Address	1	1	0	0	0	0/1	0/1	0	ACK
FM_Frequency Information	⓪	N_{14}	N_{13}	N_{12}	N_{11}	N_{10}	N_9	N_8	ACK
FL_Frequency Information	N_7	N_6	N_5	N_4	N_3	N_2	N_1	N_0	ACK
CO_Information	①	T_{14}	T_{13}	T_{12}	T_{11}	T_{10}	T_9	T_8	ACK
BA_Band Information	X	X	X	X	B_3	B_2	B_1	B_0	ACK

Chip Address

The chip address is programmable by Pin 16 (AS – Address Select).

AS – Pin 16	Address (HEX.)
Gnd to 0.1 V_{CC1}	C0
Open or 0.2 V_{CC1} to 0.3 V_{CC1}	C2
0.4 V_{CC1} to 0.7 V_{CC1}	C4
0.8 V_{CC1} to 1.1 V_{CC1}	C6

Bits B_0, B_1, B_2, B_3: Control the Band Buffers

B_0, B_1, B_2, B_3 = 0	Buffer "Off"
= 1	Buffer "On"

Figure 3. Equivalent Circuit of the Integrated Band Buffers
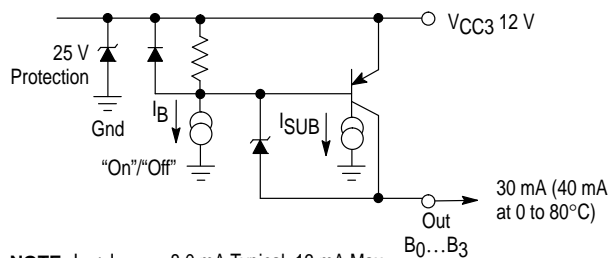
NOTE: I_B + I_{SUB} = 8.0 mA Typical, 13 mA Max
I_B = Base Current
I_{SUB} = Substrate Current of PNP

Bit T_8: Controls the Output of the Operational Amplifier

T_8 = 0	Normal Operation Operational Amplifier Active
= 1	Output State of Operational Amplifier Switched "Off", Output Pulls High Through 20 k Internal Pull–Up Resistor

Bits T_9, T_{12}: Control the Phase Comparator

T_9	T_{12}	Function
1	0	Normal Operation
1	1	High Impedance
0	0	Upper Source "On" Only
0	1	Lower Source "On" Only

Bits T_{10}, T_{11}: Control the Reference Ratio

T_{10}	T_{11}	Division Ratio
0	0	512
0	1	1024
1	0	1024
1	1	512

Bit T_{13}: Switches the Internal Signals F_{ref} and F_{BY2} to the Band Buffer Outputs (Test)

T_{13} = 0	Normal Operation
= 1	Test Mode F_{ref} Output at B_2 (Pin 12) F_{BY2} Output at B_3 (Pin 13)

Bits B_2 and B_3 have to be "On", B_2 = B_3 = 1 in the test mode.
F_{ref} is the reference frequency.
F_{BY2} is the output frequency of the programmable divider, divided by two.

Bit T_{14}: Controls the Charge Pump Current of the Phase Comparator

$T_{14} = 0$	Pump Current 15 μA Typical
= 1	Pump Current 50 μA Typical

The Programmable Divider

The programmable divider is a presettable down counter. When it has counted to zero it takes its required division ratio out of the latches B. Latches B are loaded from latches A by means of signal TDI which is synchronous to the programmable divider output signal.

Since latches A receive the data asynchronously with the programmable divider; this double latch scheme is needed to assure correct data transfer to the counter.

The division ratio definition is given by:

$N = 16384 \times N_{14} + 8192 \times N_{13} + \ldots + 4 \times N_2 + 2 \times N_1 + N_0$

Maximum Ratio 32767

Minimum Ratio 17

$N_0 \ldots N_{14}$ are the different bits for frequency information.

At power "on" the whole bus receiver is reset and the programmable divider is set to a counting ratio of N = 256 or higher.

The Prescaler

The prescaler has a preamplifier which guarantees high input sensitivity.

The Phase Comparator

The phase comparator is phase and frequency sensitive and has very low output leakage current in the high impedance state.

Lock Detector

The lock detector output is low in lock. The output goes immediately high when an unlock condition is detected. The output goes low again when the loop is in lock during a complete period of the reference frequency.

Figure 4. Equivalent Circuit of the Lock Output
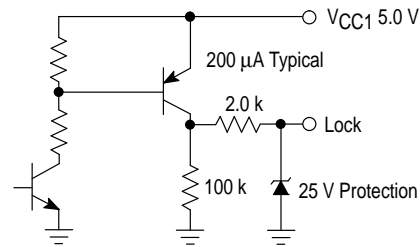
The Operational Amplifier

The operational amplifier is designed for very low noise, low input bias current and high power supply rejection. The positive input is biased internally. The operational amplifier needs 28.5 V supply (V_{CC2}) as minimum voltage for a guaranteed maximum tuning voltage of 28 V.

Figure NO TAG shows a possible filter arrangement. The component values depend very much on the application (tuner characteristic, reference frequency, etc.).

The Oscillator

The oscillator uses a 3.2 to 4.0 MHz crystal tied to ground in series with a capacitor. The crystal operates in the series resonance mode.
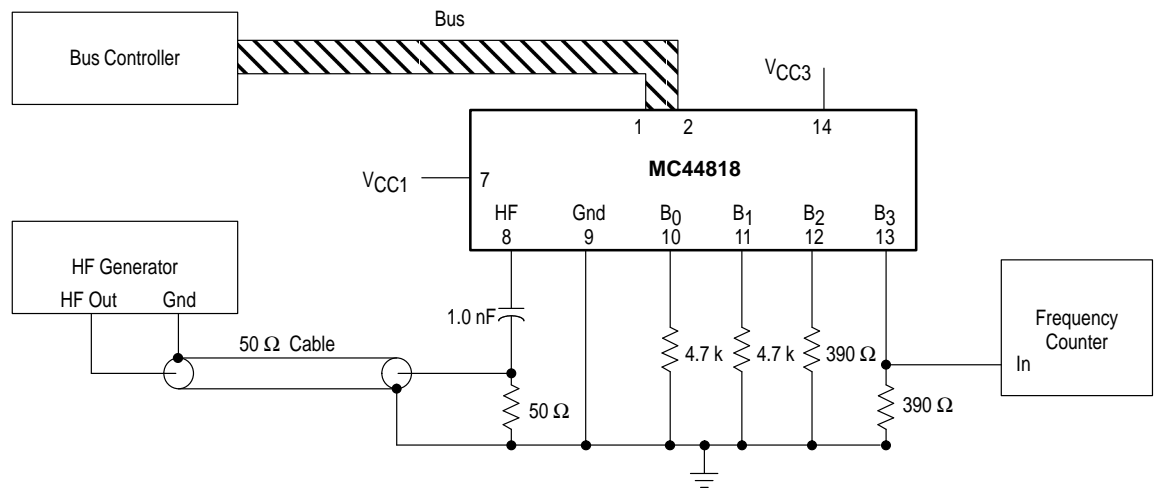
The voltage at Pin 3 has low amplitude and low harmonic distortion.

Figure 5. Typical Tuner Application

NOTES: 1. On some layouts the 100 Ω resistor will not be required.
2. C_2 = 330 pF minimum is required for stability.
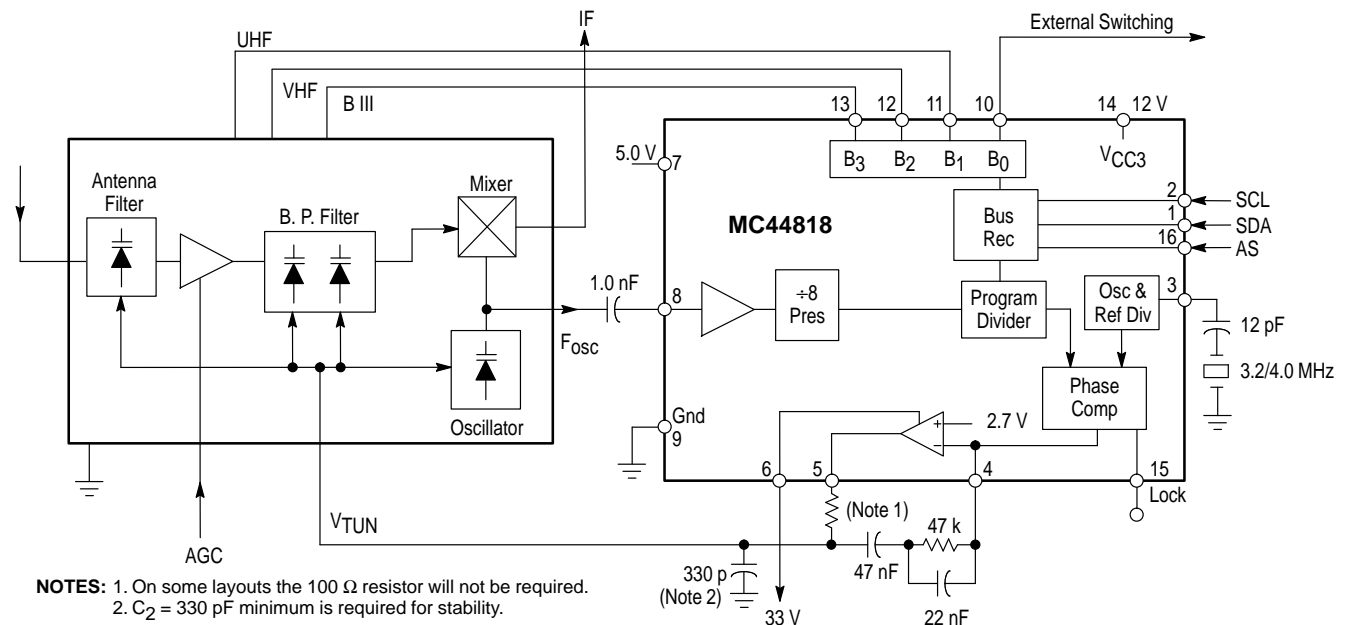
Figure 6. HF Sensitivity Test Circuit

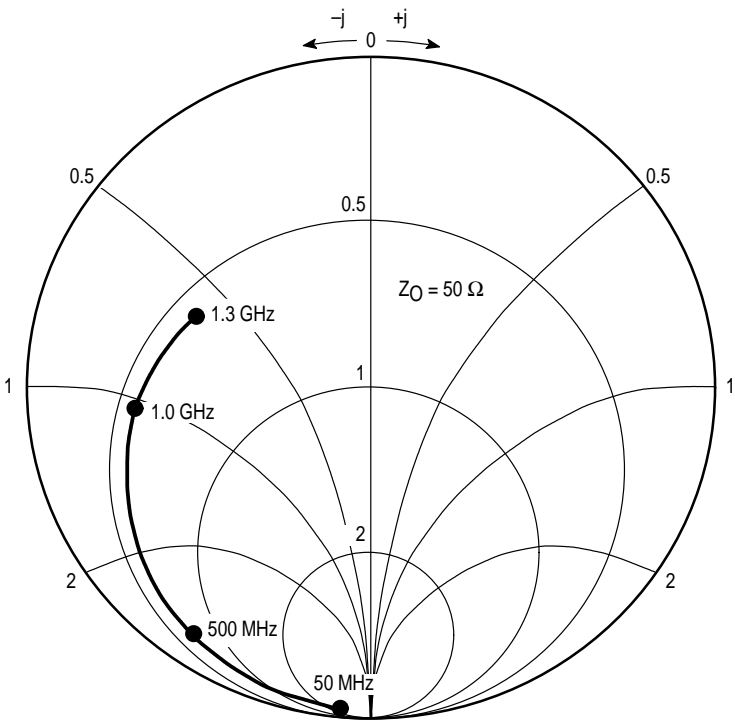
Device is in test mode. B_2, B_3 are "On" and B_0, B_1 are "Off".
Sensitivity is level of HF generator on 50 Ω load (without Pin 8 loading).
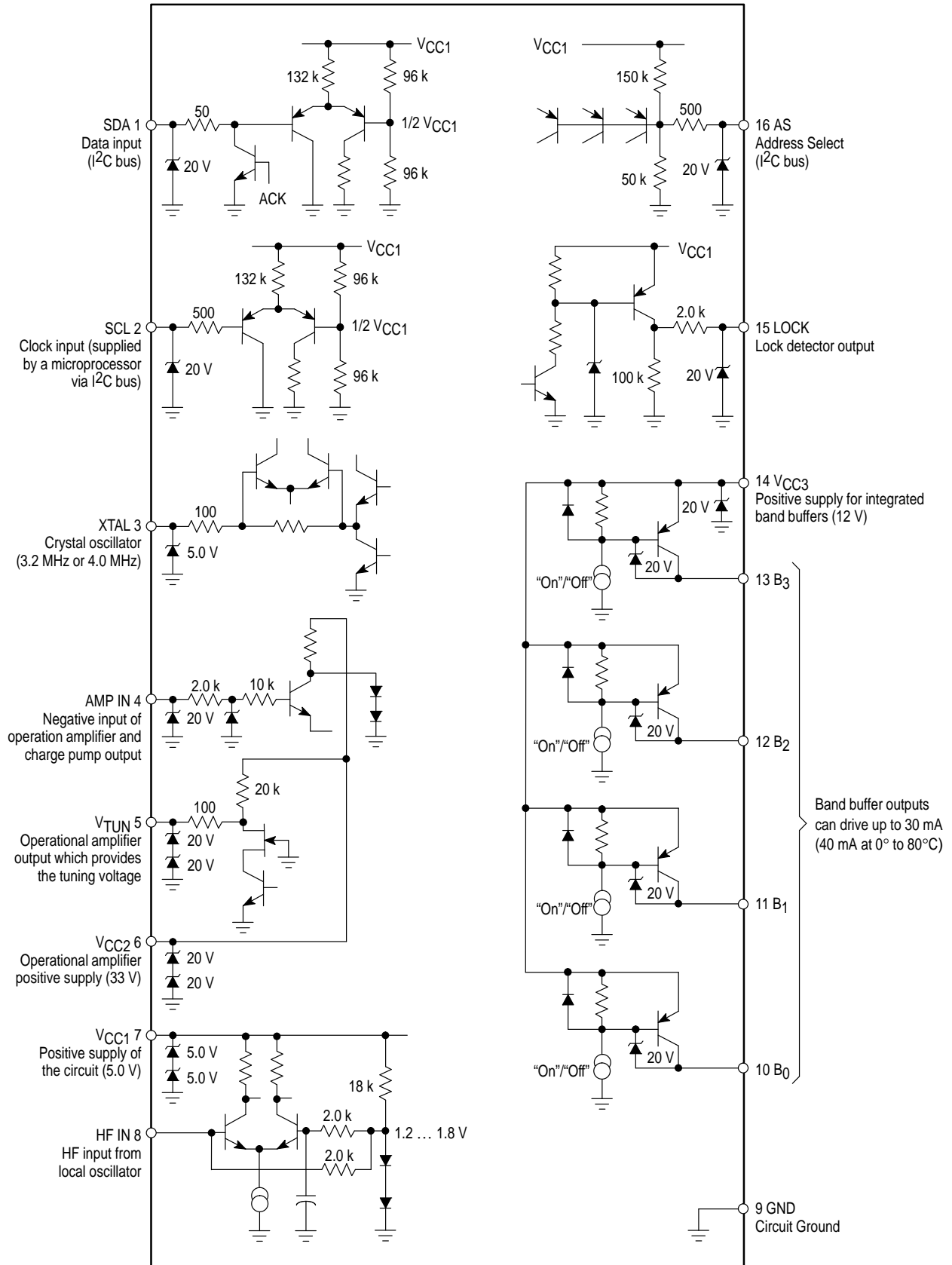
HF CHARACTERISTICS (See Figure NO TAG)

Characteristic	Pin	Min	Typ	Max	Unit
DC Bias	8	–	1.6	–	V
Input Voltage Range					mVrms
80–150 MHz	8	10	–	315	
150–600 MHz	8	5.0	–	315	
600–950 MHz	8	10	–	315	
950–1300 MHz	8	50	–	315	

Figure 7. Typical HF Input Impedance

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Figure 8. Pin Circuit Schematic

OUTLINE DIMENSIONS

D SUFFIX
PLASTIC PACKAGE
CASE 751B–05
(SO–16)
ISSUE J
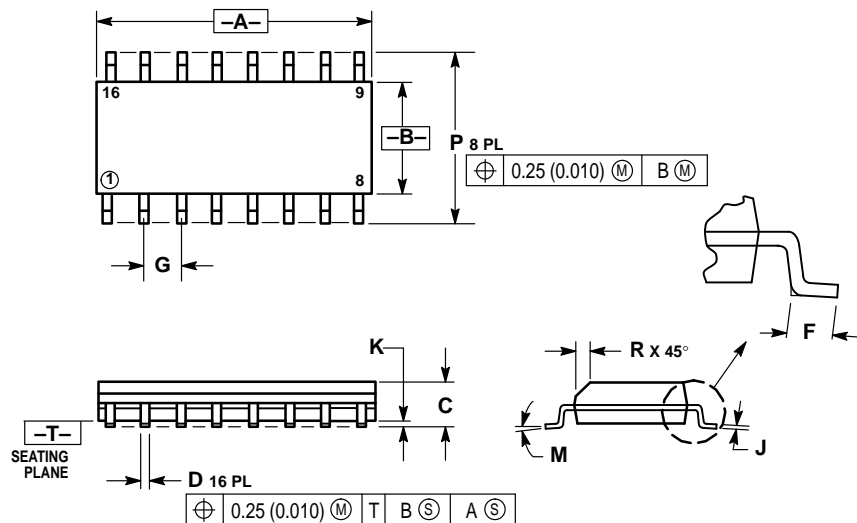
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

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