

DATA SHEET

TDA8580

Multi-purpose power amplifier

Preliminary specification
Supersedes data of 1996 Jan 4
File under Integrated Circuits, IC01

1998 Feb 25

Multi-purpose power amplifier

TDA8580

FEATURES

General

- Operating voltage from 8 to 28 V
- Low distortion
- Few external components, fixed gain
- High output power
- Can be used as a stereo amplifier in bridge-tied load (BTL) or quad single-ended (SE) amplifiers
- Single-ended mode without loudspeaker capacitor
- Mute and standby mode with one- or two-pin operation
- Diagnostic information for Dynamic Distortion Detector (DDD), high temperature (145 °C) and short-circuit
- No switch on/off plops when switching between 'standby' to 'mute' and from 'mute' to 'on'
- Low offset variation at outputs between 'mute' and 'on'
- Fast mute on supply voltage drops.

Protection

- Reverse polarity safe
- Short-circuit proof to ground, positive supply voltage on all pins and across load
- ESD protected on all pins
- Thermal protection against temperatures exceeding 150 °C
- Load dump protection
- Protected against open-circuit ground pins and output short-circuited to supply ground.

GENERAL DESCRIPTION

The TDA8580 is a stereo bridge-tied load (BTL) or a quad single-ended amplifier that operates over a wide supply voltage range from 8 to 28 V. This makes it suitable for many applications, such as car radios, television and home-sound systems.

Because of an internal voltage buffer, this device can be used without a capacitor connected in series with the load (SE application). A combined BTL and 2 × SE application can also be configured.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8580	DBS17P	plastic DIL-bent-SIL power package; 17 leads (lead length 12 mm)	SOT243-1

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QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	operating supply voltage		8.0	–	28	V
$I_{q(\text{tot})}$	total quiescent current	$V_P = 14.4 \text{ V}$	–	120	140	mA
I_{stb}	standby supply current	$V_P = 14.4 \text{ V}$	–	1	50	μA
G_V	voltage gain	single-ended	25	26	27	dB
		bridge-tied load	31	32	33	dB
Bridge-tied load application						
P_o	output power	THD = 0.5%; $V_P = 14.4 \text{ V}$; $R_L = 4 \Omega$	–	16	–	W
		THD = 0.5%; $V_P = 24 \text{ V}$; $R_L = 8 \Omega$	–	28	–	W
THD	total harmonic distortion	$f_i = 1 \text{ kHz}$; $P_o = 1 \text{ W}$; $V_P = 14.4 \text{ V}$; $R_L = 4 \Omega$	–	0.05	–	%
		$f_i = 1 \text{ kHz}$; $P_o = 10 \text{ W}$; $V_P = 24 \text{ V}$; $R_L = 8 \Omega$	–	0.05	–	%
$V_{\text{offset(DC)}}$	DC output offset voltage	$V_P = 14.4 \text{ V}$; 'mute' condition; $R_L = 4 \Omega$	–	10	20	mV
		$V_P = 14.4 \text{ V}$; 'on' condition	–	0	100	mV
V_{no}	noise output voltage	$R_S = 1 \text{ k}\Omega$; $V_P = 14.4 \text{ V}$	–	100	150	μV
SVRR	supply voltage ripple rejection	$f_i = 1 \text{ kHz}$; $V_{\text{ripple(p-p)}} = 2 \text{ V}$; 'on' or 'mute' condition; $R_S = 0 \Omega$	55	–	–	dB
Single-ended application						
P_o	output power	THD = 0.5%; $V_P = 14.4 \text{ V}$; $R_L = 4 \Omega$	–	4.2	–	W
		THD = 0.5%; $V_P = 24 \text{ V}$; $R_L = 4 \Omega$	–	13	–	W
$V_{\text{offset(DC)}}$	DC output offset voltage	$V_P = 14.4 \text{ V}$; 'mute' condition; $R_L = 4 \Omega$	–	10	20	mV
		$V_P = 14.4 \text{ V}$; 'on' condition	–	0	100	mV
V_{no}	noise output voltage	$R_S = 1 \text{ k}\Omega$; $V_P = 14.4 \text{ V}$	–	80	120	μV
SVRR	supply voltage ripple rejection	$f_i = 1 \text{ kHz}$; $V_{\text{ripple(p-p)}} = 2 \text{ V}$; 'on' or 'mute' condition; $R_S = 0 \Omega$	45	–	–	dB

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BLOCK DIAGRAM

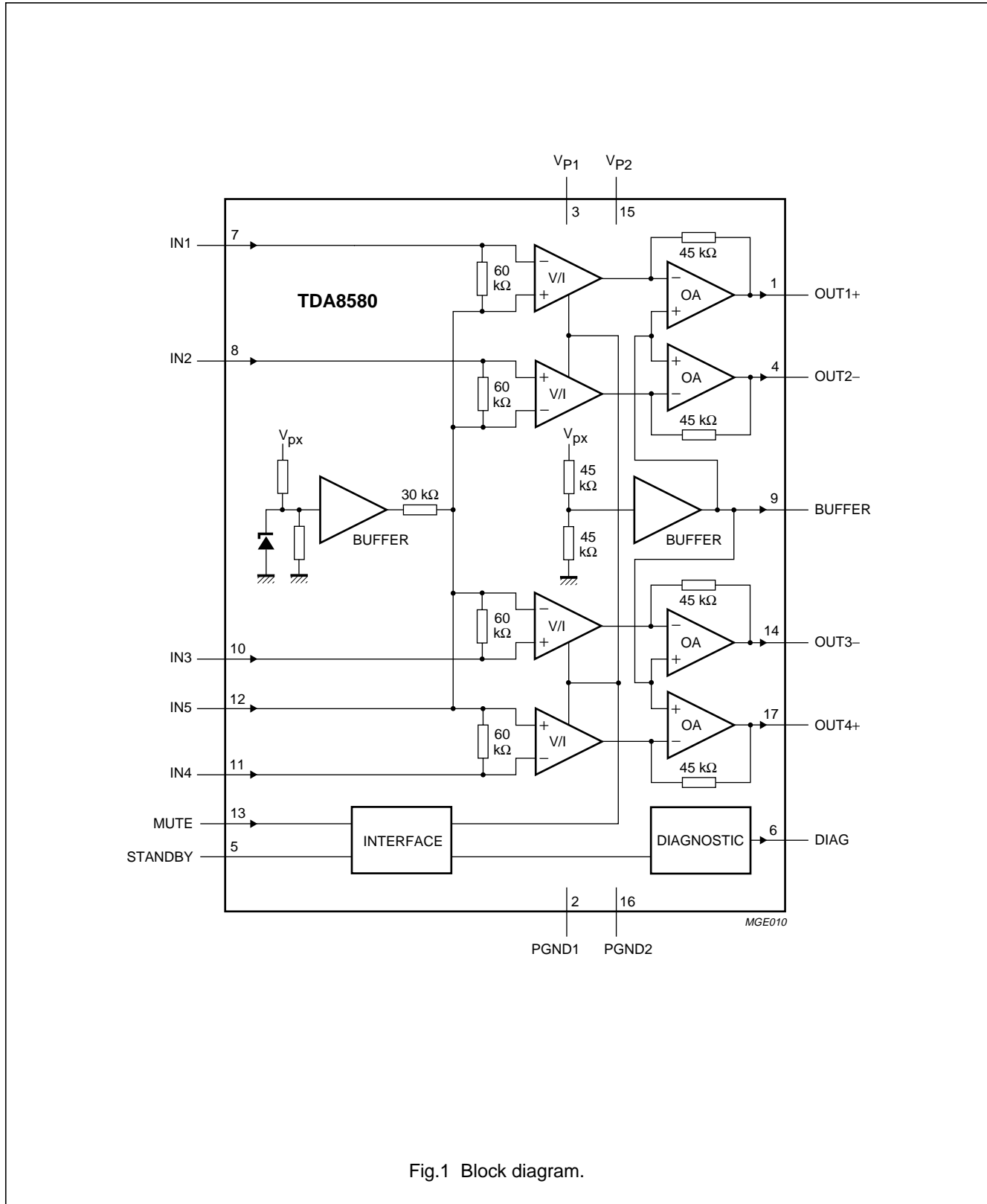


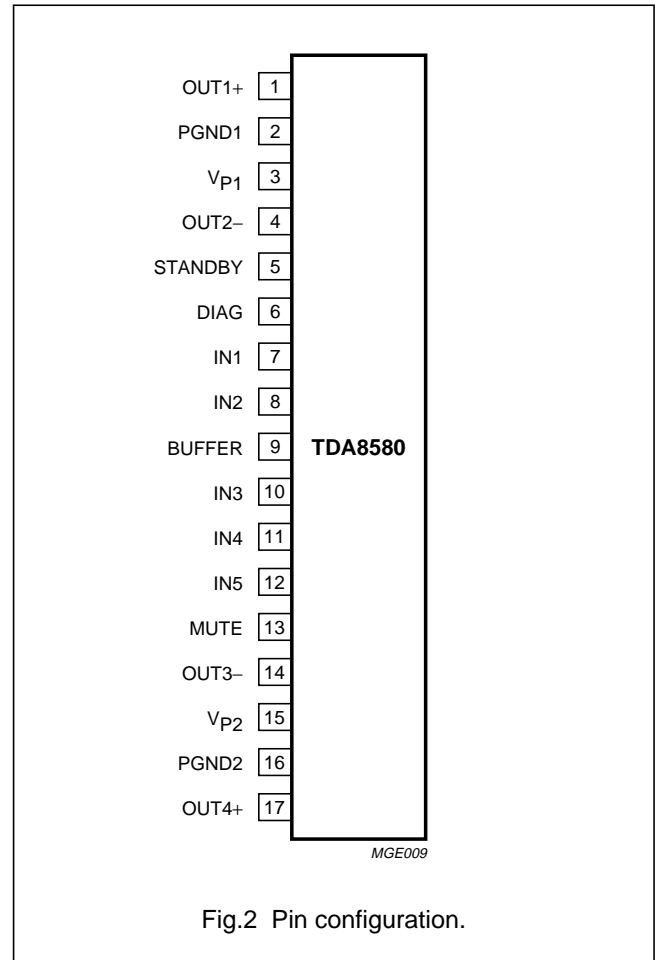
Fig.1 Block diagram.

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PINNING

SYMBOL	PIN	DESCRIPTION
OUT1+	1	non-inverting output 1
PGND1	2	power ground 1
V _{P1}	3	supply voltage 1
OUT2-	4	inverting output 2
STANDBY	5	'standby'/'mute'/'on' selection
DIAG	6	diagnostic output
IN1	7	input 1
IN2	8	input 2
BUFFER	9	buffer output (single-ended output buffer)
IN3	10	input 3
IN4	11	input 4
IN5	12	input 5; signal ground capacitor
MUTE	13	'mute'/'on' selection
OUT3-	14	inverting output 3
V _{P2}	15	supply voltage 2
PGND2	16	power ground 2
OUT4+	17	non-inverting output 4



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FUNCTIONAL DESCRIPTION

The TDA8580 is a multi-purpose power amplifier with four amplifiers which can be connected in the following configurations with high output power and low distortion (at minimum quiescent current);

- Dual bridge-tied load (BTL) amplifiers
- Quad single-ended amplifiers
- Dual single-ended amplifiers and one bridge-tied load amplifier.

The amplifier can be switched on (play or 'mute') and off ('standby') by the MUTE and STANDBY pins (for interfacing directly with a microcontroller). One-pin operation is also possible by applying a voltage greater than 8 V to the 'standby'/'mute'/'on' selection pin (pin 5) to switch the amplifier in 'on' mode.

Special attention is given to the dynamic behaviour as follows:

- Noise suppression during engine start.
- No pops when switching from 'standby' to 'on'.
- Slow offset change between 'mute' and 'on' (controlled by MUTE and STANDBY pins).
- Low noise levels, which are independent of the supply voltage.

Protections are included to avoid the IC being damaged at:

- Over temperature: $T > 150\text{ }^{\circ}\text{C}$.
- Short-circuit of the output pin(s) to ground or supply rail. When short-circuited, the power dissipation is limited.
- A missing-current limiter which limits the maximum short circuit output current to PGND or V_P pins to 1 A. The dissipation and speaker current will be minimized because the short-circuited amplifier is switched off. The chip temperature is limited by the temperature protection.
- ESD protection (Human Body Model 3000 V, Machine Model 300 V).
- Energy handling. A DC voltage of 6 V can be connected to the output of any amplifier while the supply pins are short-circuited to ground. No high DC current will flow from the supply pins of the amplifier.

Diagnostics are available for the following conditions (see Figs 4 to 7).

- Amplifier in 'mute'
- Chip temperature greater than $145\text{ }^{\circ}\text{C}$
- Distortion over 2% due to clipping
- Short-circuit protection active.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_P	supply voltage	operating	8	28	V
		load dump protected; see Fig.3	–	45	V
V_{DIAG}	voltage on diagnostic pin		–	18	V
I_{OSM}	non-repetitive peak output current		–	6	A
I_{ORM}	repetitive peak output current		–	4.5	A
V_{rev}	reverse polarity voltage		–	6	V
V_{sc}	AC and DC short-circuit voltage of output pins across loads and to ground or supply pins	no external series resistor in supply line; note 1	–	24	V
P_{tot}	total power dissipation		–	75	W
T_j	junction temperature		–	150	$^{\circ}\text{C}$
T_{stg}	storage temperature		–55	+150	$^{\circ}\text{C}$
T_{amb}	operating ambient temperature		–40	+150	$^{\circ}\text{C}$

Note

1. The maximum supply voltage under short circuit conditions is 28 V with an additional resistor in the supply line of $\text{tbf } \Omega$.

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THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j-a}$	thermal resistance from junction to ambient	in free air	40	K/W
$R_{th\ j-c}$	thermal resistance from junction to case		1.5	K/W

CHARACTERISTICS

$V_P = 14.4\text{ V}$; $T_{amb} = 25\text{ °C}$; $f_i = 1\text{ kHz}$; $R_L = \infty$; measured in test circuit of Fig.8; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_P	operating supply voltage		8.0	14.4	28	V
$I_{q(tot)}$	total quiescent current		–	120	140	mA
I_{stb}	standby current		–	1	50	μA
V_O	DC output voltage	$V_P = 14.4\text{ V}$	–	7.0	–	V
$V_{P(mute)}$	low supply voltage mute		6.0	7.0	8.0	V
V_o	single-ended and bridge-tied load output voltage	$V_P = 14.4\text{ V}$; 'mute' condition; $R_L = 4\ \Omega$	–	–	20	mV
V_I	DC input voltage	$V_P = 14.4\text{ V}$	–	4.0	–	V
STANDBY PIN (see Table 1)						
$V_{5(stb)}$	voltage at STANDBY pin for 'standby' condition		0	–	0.8	V
$V_{hys(5)(stb)}$	hysteresis voltage at STANDBY pin for 'standby' condition	note 1	–	0.2	–	V
$V_{5(mute)}$	voltage at STANDBY pin for 'mute' condition	$V_{13} < 1\text{ V}$	2.0	–	5.5	V
$V_{5(on)}$	voltage at STANDBY pin for 'on' condition	$V_{13} < 1\text{ V}$; $V_P > 9\text{ V}$; note 2	8.0	–	18	V
MUTE PIN (see Table 1)						
$V_{13(mute)}$	voltage at MUTE pin for 'mute' condition	$V_5 = 5\text{ V}$	0	–	1.0	V
$V_{13(on)}$	voltage at MUTE pin for 'on' condition	$V_5 = 5\text{ V}$	3.5	–	5.5	V
Diagnostic; output buffer (open-collector); see Figs 4, 5, 6 and 7						
V_{OL}	low level output voltage	$I_{sink} = 1\text{ mA}$	–	0.2	0.8	V
I_{LI}	leakage current	$V_{DIAG} = 14.4\text{ V}$	–	–	1	μA
CD	clip detector	$V_{DIAG} < 0.8\text{ V}$	tbf	2	tbf	%
$T_{j(diag)}$	junction temperature for high temperature warning	$V_{DIAG} < 0.8\text{ V}$	–	145	–	$^{\circ}\text{C}$

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Stereo BTL application (see Fig.8)						
THD	total harmonic distortion	$f_i = 1 \text{ kHz}; P_o = 1 \text{ W}; R_L = 4 \Omega$	–	0.05	0.1	%
		$f_i = 10 \text{ kHz}; P_o = 1 \text{ W}; R_L = 4 \Omega;$ Filter: $22 \text{ Hz} < f < 30 \text{ kHz}$	–	0.2	–	%
		$f_i = 1 \text{ kHz}; P_o = 1 \text{ W}; V_P = 14.4 \text{ V}; R_L = 4 \Omega$	–	0.05	–	%
		$f_i = 1 \text{ kHz}; P_o = 10 \text{ W}; V_P = 24 \text{ V}; R_L = 8 \Omega$	–	0.05	–	%
P_o	output power	THD = 0.5%; $V_P = 14.4 \text{ V}; R_L = 4 \Omega$	15	16	–	W
		THD = 0.5%; $V_P = 24 \text{ V}; R_L = 8 \Omega$	25	28	–	W
		THD = 10%; $V_P = 14.4 \text{ V}; R_L = 4 \Omega$	18	20	–	W
		THD = 10%; $V_P = 24 \text{ V}; R_L = 8 \Omega$	–	35	–	W
G_v	voltage gain	$V_{o(rms)} = 3 \text{ V}$	31	32	33	dB
α_{cs}	channel separation	$P_o = 2 \text{ W}; f_i = 1 \text{ kHz}; R_L = 4 \Omega$	40	55	–	dB
$ \Delta G_v $	channel unbalance		–	–	1	dB
$V_{offset(DC)}$	DC output offset voltage	$V_P = 14.4 \text{ V};$ 'on' condition	–	0	100	mV
		$V_P = 14.4 \text{ V};$ 'mute' condition; $R_L = 4 \Omega$	–	10	20	mV
V_{no}	noise output voltage	$R_s = 1 \text{ k}\Omega; V_P = 14.4 \text{ V};$ note 3	–	100	150	μV
$V_{no(mute)}$	noise output voltage mute	note 3	–	0	20	μV
$V_{o(mute)}$	output voltage mute	$V_{i(rms)} = 1 \text{ V}$	–	3	500	μV
SVRR	supply voltage ripple rejection	$R_s = 0 \Omega; f_i = 1 \text{ kHz}; V_{ripple(p-p)} = 2 \text{ V};$ 'on' or 'mute' condition	55	–	–	dB
Z_i	input impedance		23	30	37	$\text{k}\Omega$
CMRR	common mode rejection ratio	$R_s = 0 \Omega; V_{i(rms)} = 0.5 \text{ V}; f_i = 1 \text{ kHz}$	–	60	–	dB
Quad SE application (see Fig.9)						
THD	total harmonic distortion	$f_i = 1 \text{ kHz}; P_o = 1 \text{ W}; R_L = 4 \Omega$	–	0.05	0.1	%
		$f_i = 10 \text{ kHz}; P_o = 1 \text{ W}; R_L = 4 \Omega;$ Filter: $22 \text{ Hz} < f < 30 \text{ kHz}$	–	0.2	–	%

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
P _o	output power	THD = 0.5%; V _P = 14.4 V; R _L = 4 Ω	4	4.2	–	W
		THD = 0.5%; V _P = 24 V; R _L = 4 Ω	11.5	13	–	W
		THD = 10%; V _P = 14.4 V; R _L = 4 Ω	–	5.5	–	W
		THD = 10%; V _P = 24 V; R _L = 4 Ω	14	16	–	W
G _v	voltage gain	V _{o(rms)} = 3 V	25	26	27	dB
α _{cs}	channel separation	P _o = 2 W; f _i = 1 kHz; R _L = 4 Ω	40	46	–	dB
ΔG _v	channel unbalance		–	–	1	dB
V _{offset(DC)}	DC output offset voltage	V _P = 14.4 V; 'on' condition	–	0	100	mV
		V _P = 14.4 V; 'mute' condition; R _L = 4 Ω	–	10	20	mV
V _{no}	noise output voltage	R _s = 1 kΩ; V _P = 14.4 V; note 3	–	80	120	μV
V _{no(mute)}	noise output voltage mute	note 3	–	0	20	μV
V _{o(mute)}	output voltage mute	V _{i(rms)} = 1 V	–	3	500	μV
SVRR	supply voltage ripple rejection	f _i = 1 kHz; V _{ripple(p-p)} = 2 V, 'on' or 'mute' condition; R _s = 0 Ω	45	–	–	dB
Z _i	input impedance		46	60	74	kΩ
CMRR	common mode rejection ratio	V _{i(rms)} = 0.5 V; f _i = 1 kHz; R _s = 0 Ω	–	60	–	dB

Notes to the characteristics

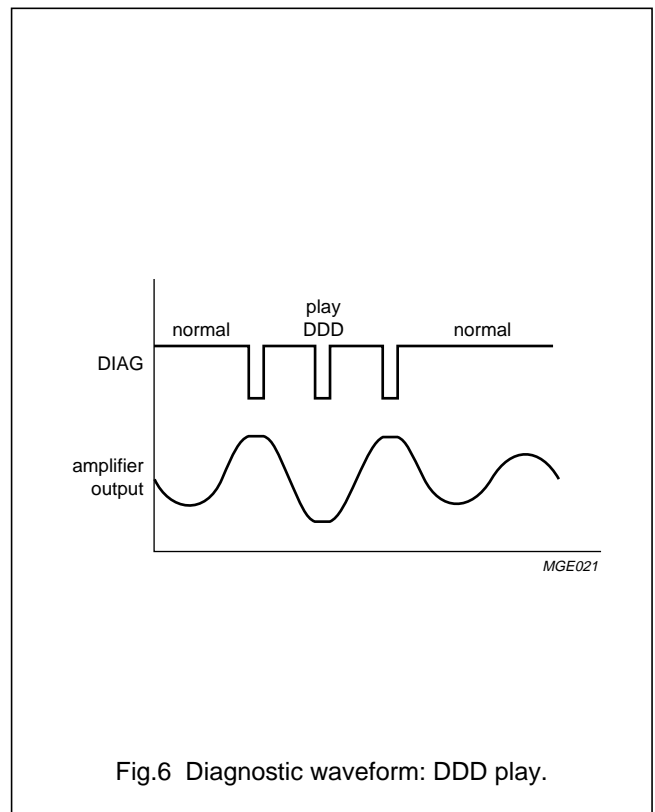
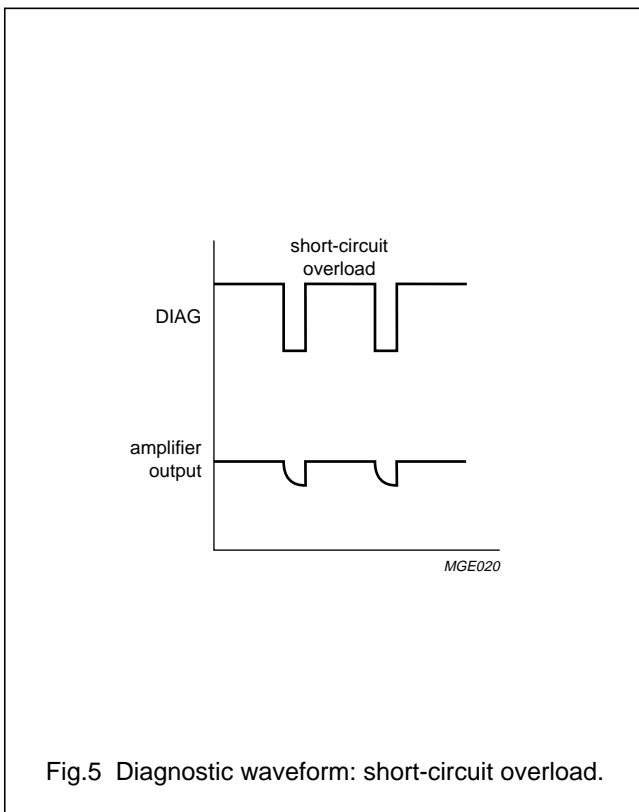
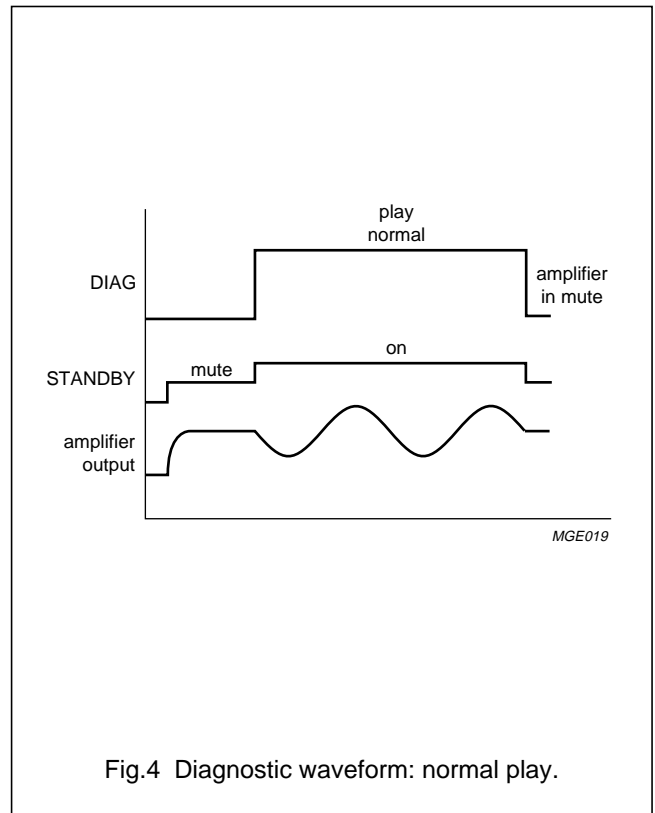
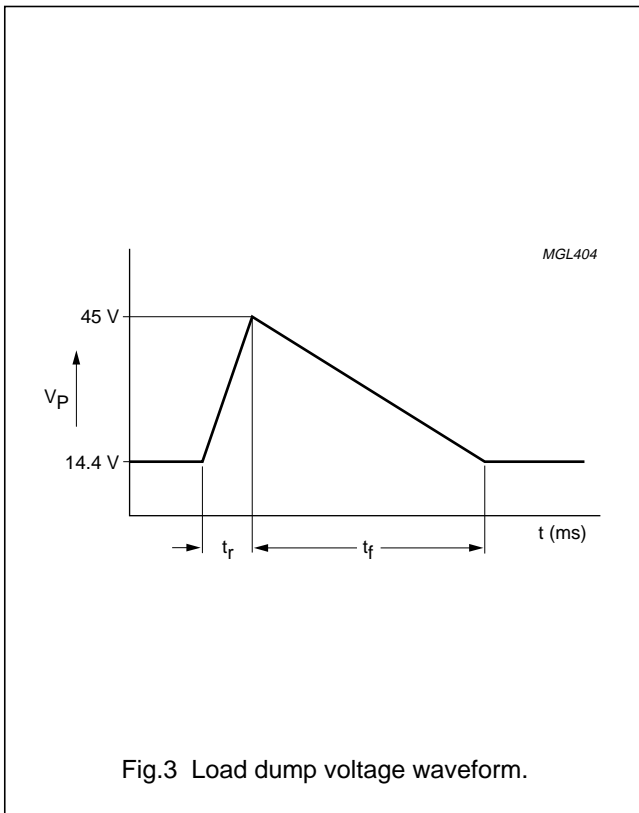
1. Hysteresis between rise and fall voltage when MSB pin is controlled with real voltage source (the hysteresis depends on resistor connected to MSB pin).
2. At lower V_P the voltage at the STANDBY pin for 'on' condition will be adjusted automatically to maintain an 'on' condition at low battery voltage (down to 8 V) when using one-pin operation.
3. The noise output is measured in a bandwidth of 20 Hz to 20 kHz.

Table 1 Selection of 'standby', 'mute' and 'on'.

VOLTAGE AT PIN 5	VOLTAGE AT PIN 13	FUNCTION
V ₅ < 0.8 V	don't care	'standby' (off)
2 V < V ₅ < 5.3 V	V ₁₃ < 1 V	'mute' (DC settled)
2 V < V ₅ < 5.3 V	3.5 V < V ₁₃ < 5.3 V	'on' (AC operating)
V ₅ ≥ 8.0 V	don't care	'on' (AC operating)

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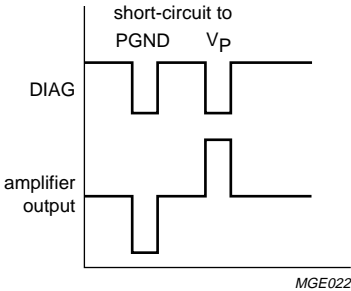


Fig.7 Diagnostic waveform: short-circuit to GND and Vp.

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APPLICATION INFORMATION

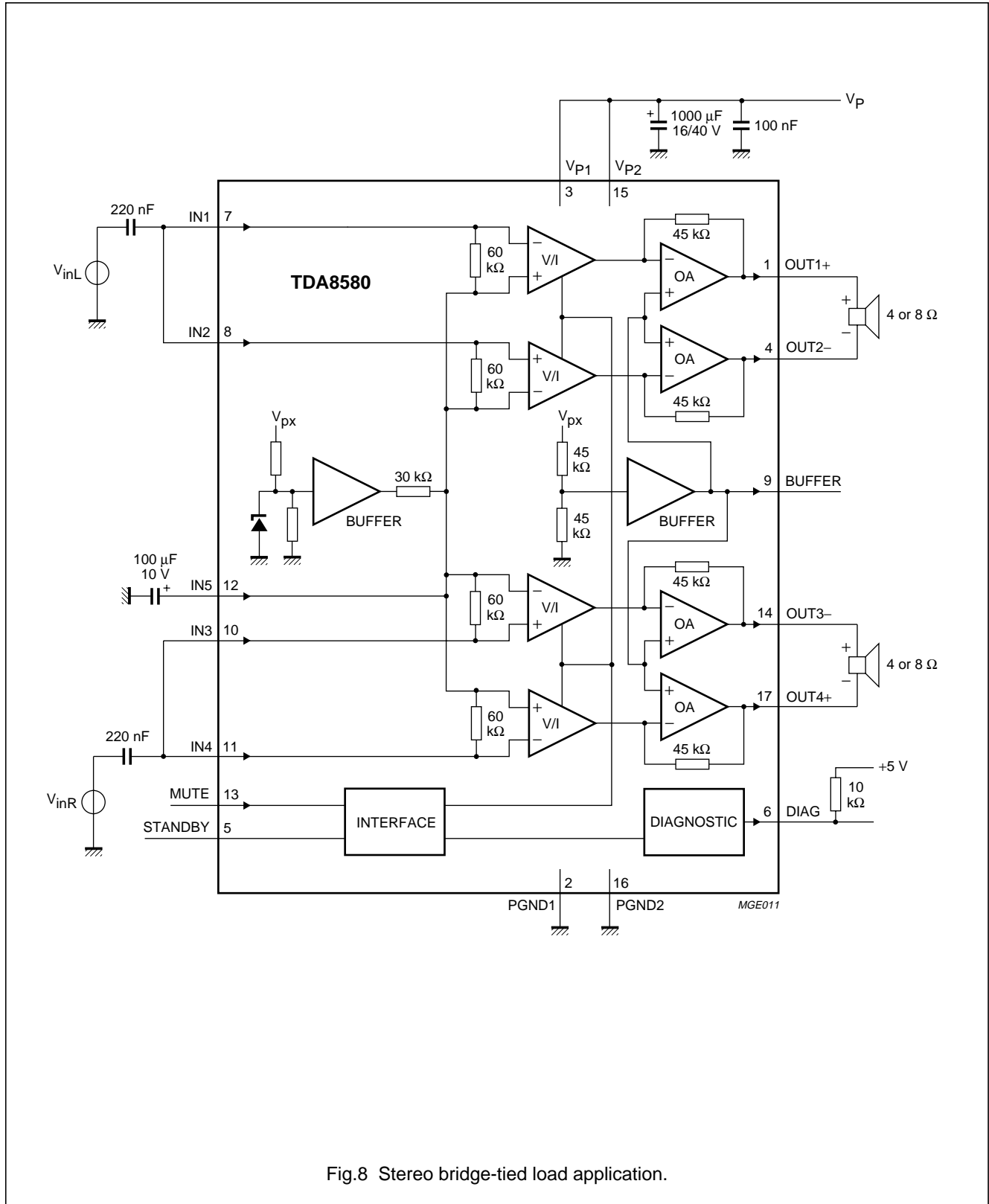


Fig.8 Stereo bridge-tied load application.

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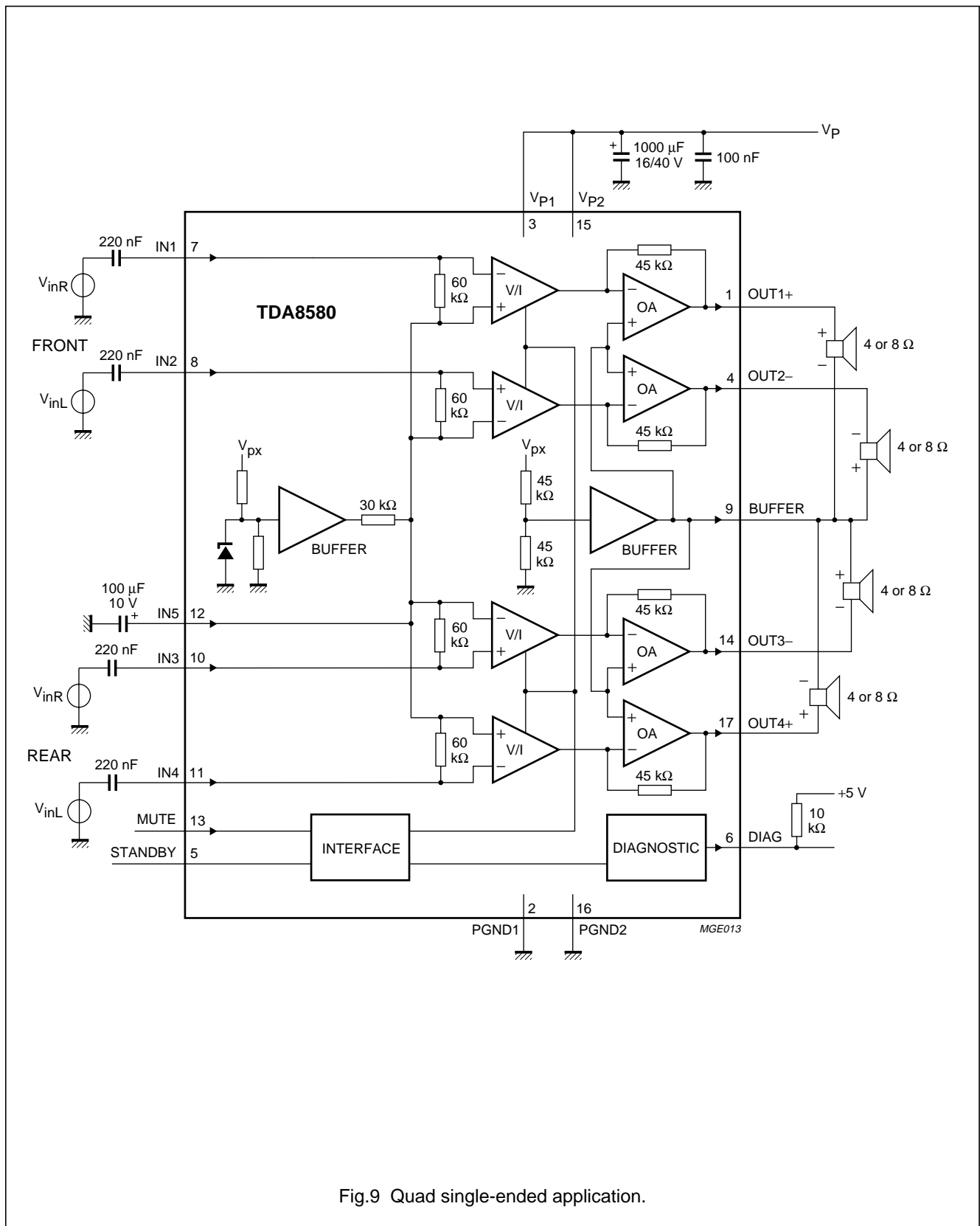


Fig.9 Quad single-ended application.

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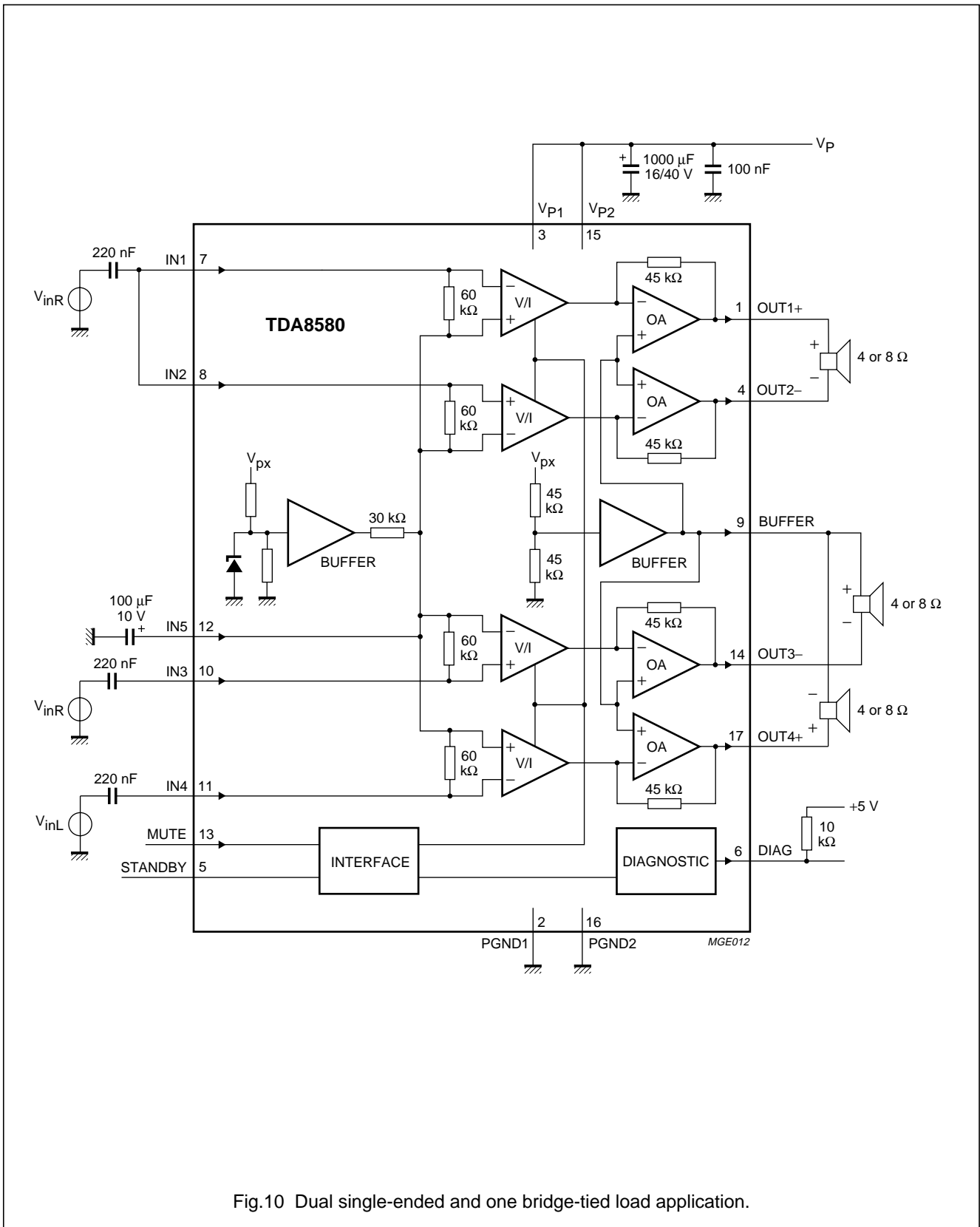


Fig.10 Dual single-ended and one bridge-tied load application.

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INTERNAL PIN CONFIGURATION

PIN	NAME	EQUIVALENT CIRCUIT
7, 8, 10, 11 and 12	inputs	
1, 4, 14 and 17	outputs	
5 and 13	mode select	

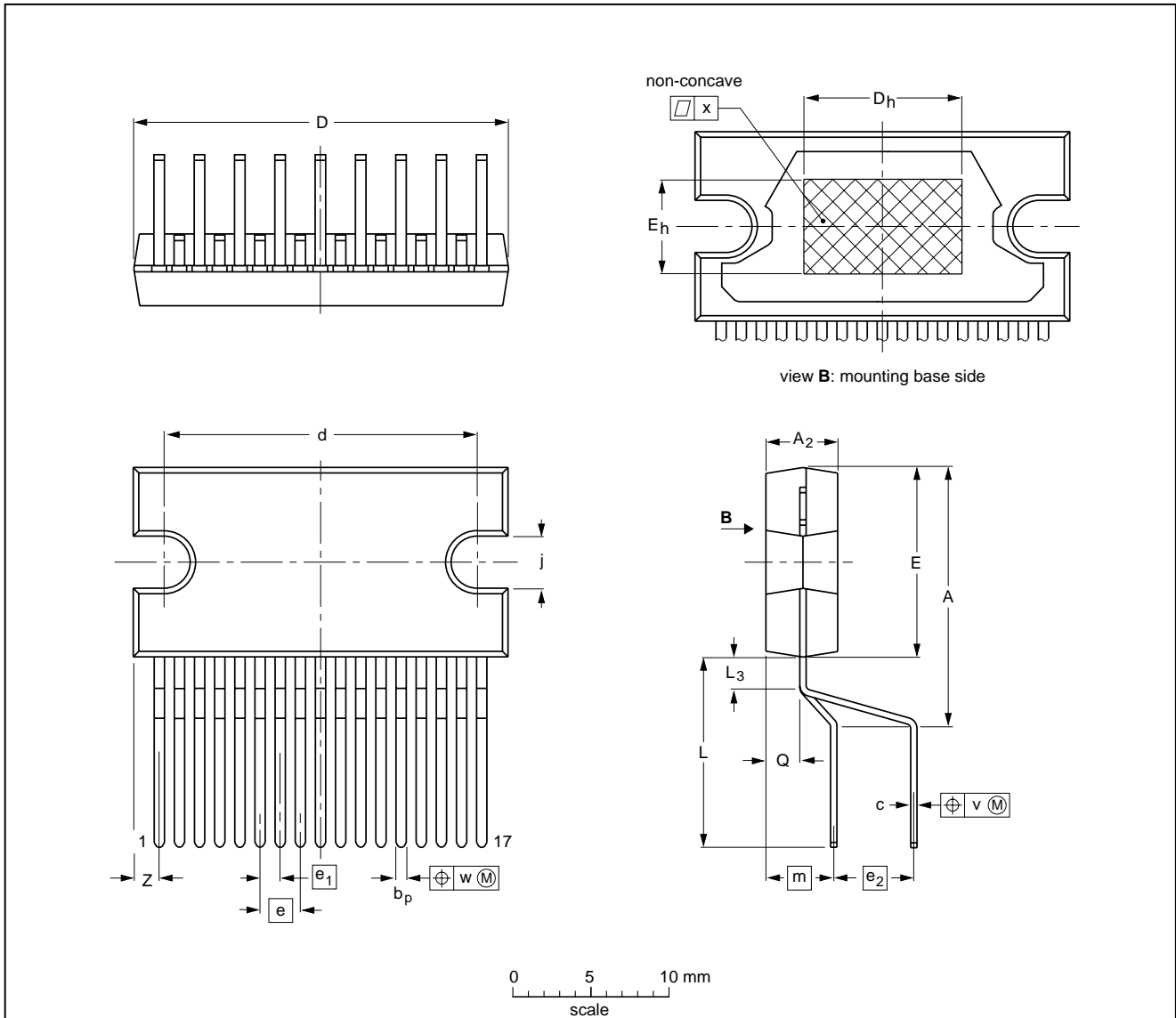
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PACKAGE OUTLINE

DBS17P: plastic DIL-bent-SIL power package; 17 leads (lead length 12 mm)

SOT243-1



DIMENSIONS (mm are the original dimensions)

UNIT	A	A ₂	b _p	c	D ⁽¹⁾	d	D _h	E ⁽¹⁾	e	e ₁	e ₂	E _h	j	L	L ₃	m	Q	v	w	x	Z ⁽¹⁾
mm	17.0 15.5	4.6 4.2	0.75 0.60	0.48 0.38	24.0 23.6	20.0 19.6	10	12.2 11.8	2.54	1.27	5.08	6	3.4 3.1	12.4 11.0	2.4 1.6	4.3	2.1 1.8	0.8	0.4	0.03	2.00 1.45

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT243-1						95-03-11 97-12-16

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SOLDERING**Introduction**

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our "IC Package Databook" (order code 9398 652 90011).

Soldering by dipping or by wave

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact

with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg\ max}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

Repairing soldered joints

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

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NOTES

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NOTES

Philips Semiconductors – a worldwide company

Argentina: see South America

Australia: 34 Waterloo Road, NORTH RYDE, NSW 2113,
Tel. +61 2 9805 4455, Fax. +61 2 9805 4466

Austria: Computerstr. 6, A-1101 WIEN, P.O. Box 213, Tel. +43 160 1010,
Fax. +43 160 101 1210

Belarus: Hotel Minsk Business Center, Bld. 3, r. 1211, Volodarski Str. 6,
220050 MINSK, Tel. +375 172 200 733, Fax. +375 172 200 773

Belgium: see The Netherlands

Brazil: see South America

Bulgaria: Philips Bulgaria Ltd., Energoproject, 15th floor,
51 James Bourchier Blvd., 1407 SOFIA,
Tel. +359 2 689 211, Fax. +359 2 689 102

Canada: PHILIPS SEMICONDUCTORS/COMPONENTS,
Tel. +1 800 234 7381

China/Hong Kong: 501 Hong Kong Industrial Technology Centre,
72 Tat Chee Avenue, Kowloon Tong, HONG KONG,
Tel. +852 2319 7888, Fax. +852 2319 7700

Colombia: see South America

Czech Republic: see Austria

Denmark: Prags Boulevard 80, PB 1919, DK-2300 COPENHAGEN S,
Tel. +45 32 88 2636, Fax. +45 31 57 0044

Finland: Sinikalliontie 3, FIN-02630 ESPOO,
Tel. +358 9 615800, Fax. +358 9 61580920

France: 51 Rue Carnot, BP317, 92156 SURESNES Cedex,
Tel. +33 1 40 99 6161, Fax. +33 1 40 99 6427

Germany: Hammerbrookstraße 69, D-20097 HAMBURG,
Tel. +49 40 23 53 60, Fax. +49 40 23 536 300

Greece: No. 15, 25th March Street, GR 17778 TAVROS/ATHENS,
Tel. +30 1 4894 339/239, Fax. +30 1 4814 240

Hungary: see Austria

India: Philips INDIA Ltd, Band Box Building, 2nd floor,
254-D, Dr. Annie Besant Road, Worli, MUMBAI 400 025,
Tel. +91 22 493 8541, Fax. +91 22 493 0966

Indonesia: see Singapore

Ireland: Newstead, Clonskeagh, DUBLIN 14,
Tel. +353 1 7640 000, Fax. +353 1 7640 200

Israel: RAPAC Electronics, 7 Kehilat Saloniki St, PO Box 18053,
TEL AVIV 61180, Tel. +972 3 645 0444, Fax. +972 3 649 1007

Italy: PHILIPS SEMICONDUCTORS, Piazza IV Novembre 3,
20124 MILANO, Tel. +39 2 6752 2531, Fax. +39 2 6752 2557

Japan: Philips Bldg 13-37, Kohnan 2-chome, Minato-ku, TOKYO 108,
Tel. +81 3 3740 5130, Fax. +81 3 3740 5077

Korea: Philips House, 260-199 Itaewon-dong, Yongsan-ku, SEOUL,
Tel. +82 2 709 1412, Fax. +82 2 709 1415

Malaysia: No. 76 Jalan Universiti, 46200 PETALING JAYA, SELANGOR,
Tel. +60 3 750 5214, Fax. +60 3 757 4880

Mexico: 5900 Gateway East, Suite 200, EL PASO, TEXAS 79905,
Tel. +9-5 800 234 7381

Middle East: see Italy

Netherlands: Postbus 90050, 5600 PB EINDHOVEN, Bldg. VB,
Tel. +31 40 27 82785, Fax. +31 40 27 88399

New Zealand: 2 Wagener Place, C.P.O. Box 1041, AUCKLAND,
Tel. +64 9 849 4160, Fax. +64 9 849 7811

Norway: Box 1, Manglerud 0612, OSLO,
Tel. +47 22 74 8000, Fax. +47 22 74 8341

Philippines: Philips Semiconductors Philippines Inc.,
106 Valero St. Salcedo Village, P.O. Box 2108 MCC, MAKATI,
Metro MANILA, Tel. +63 2 816 6380, Fax. +63 2 817 3474

Poland: Ul. Lukiska 10, PL 04-123 WARSZAWA,
Tel. +48 22 612 2831, Fax. +48 22 612 2327

Portugal: see Spain

Romania: see Italy

Russia: Philips Russia, Ul. Usatcheva 35A, 119048 MOSCOW,
Tel. +7 095 755 6918, Fax. +7 095 755 6919

Singapore: Lorong 1, Toa Payoh, SINGAPORE 1231,
Tel. +65 350 2538, Fax. +65 251 6500

Slovakia: see Austria

Slovenia: see Italy

South Africa: S.A. PHILIPS Pty Ltd., 195-215 Main Road Martindale,
2092 JOHANNESBURG, P.O. Box 7430 Johannesburg 2000,
Tel. +27 11 470 5911, Fax. +27 11 470 5494

South America: Al. Vicente Pinzon, 173, 6th floor,
04547-130 SÃO PAULO, SP, Brazil,
Tel. +55 11 821 2333, Fax. +55 11 821 2382

Spain: Balmes 22, 08007 BARCELONA,
Tel. +34 3 301 6312, Fax. +34 3 301 4107

Sweden: Kottbygatan 7, Akalla, S-16485 STOCKHOLM,
Tel. +46 8 632 2000, Fax. +46 8 632 2745

Switzerland: Allmendstrasse 140, CH-8027 ZÜRICH,
Tel. +41 1 488 2686, Fax. +41 1 488 3263

Taiwan: Philips Semiconductors, 6F, No. 96, Chien Kuo N. Rd., Sec. 1,
TAIPEI, Taiwan Tel. +886 2 2134 2865, Fax. +886 2 2134 2874

Thailand: PHILIPS ELECTRONICS (THAILAND) Ltd.,
209/2 Sanpavuth-Bangna Road Prakanong, BANGKOK 10260,
Tel. +66 2 745 4090, Fax. +66 2 398 0793

Turkey: Talatpasa Cad. No. 5, 80640 GÜLTEPE/ISTANBUL,
Tel. +90 212 279 2770, Fax. +90 212 282 6707

Ukraine: PHILIPS UKRAINE, 4 Patrice Lumumba str., Building B, Floor 7,
252042 KIEV, Tel. +380 44 264 2776, Fax. +380 44 268 0461

United Kingdom: Philips Semiconductors Ltd., 276 Bath Road, Hayes,
MIDDLESEX UB3 5BX, Tel. +44 181 730 5000, Fax. +44 181 754 8421

United States: 811 East Arques Avenue, SUNNYVALE, CA 94088-3409,
Tel. +1 800 234 7381

Uruguay: see South America

Vietnam: see Singapore

Yugoslavia: PHILIPS, Trg N. Pasica 5/v, 11000 BEOGRAD,
Tel. +381 11 625 344, Fax. +381 11 635 777

For all other countries apply to: Philips Semiconductors,
International Marketing & Sales Communications, Building BE-p, P.O. Box 218,
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