Preliminary Product Specification - 12th September, 1997.

STR-F6600 Series

Allegro Microsystems Europe Ltd.

Sanken

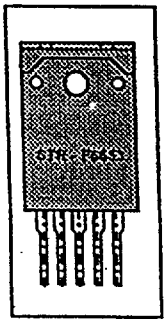
SMPS PRIMARY IC.

Advantages

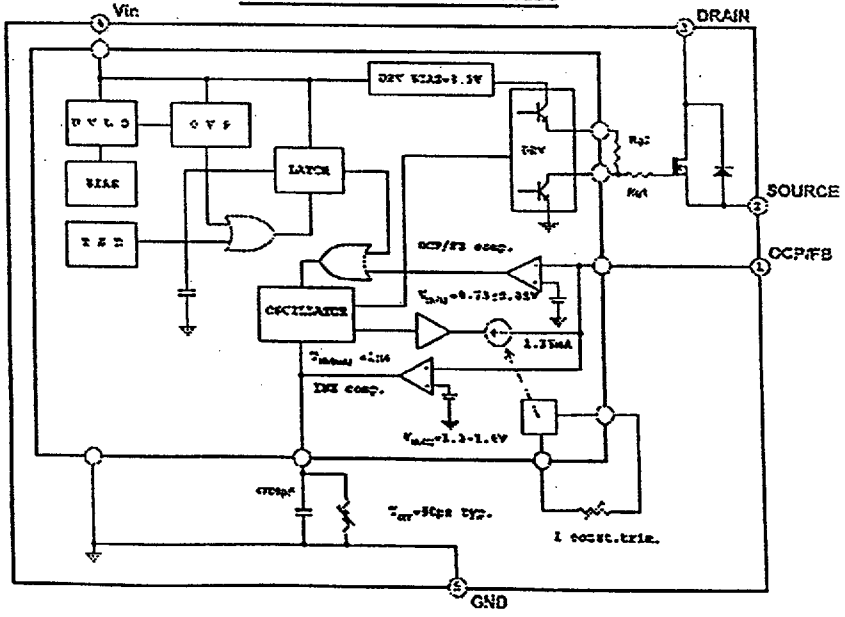
- Greatly Reduced Parts Count
- Rugged Avalanche Rated MOSFET
- Choice of MOSFET Voltage and Rds(on)
- Flyback Operation with Quasi-Resonant Soft Switching for Low Dissipation & EMI
- Full Overcurrent Protection (no blanking)
- Undervoltage Lock-out with Hysteresis
- Overvoltage Protection
- Direct Voltage Feedback
- Low Start-up current, <400uA
- Low Frequency Low power Standby Operation
- Rugged Isolated 5 pin Package

The STR-F6600 series from Allegro/ Sanken is a range of low cost, offline hybrid IC regulators covering applications from 20 to 300 watt.

This flexibility is achieved by offering a choice of MOSFET Rdson and VOS ratings. A very high performance regulator and MOSFET, together with internal trimming, keep external parts count very low without compromising regulator performance.



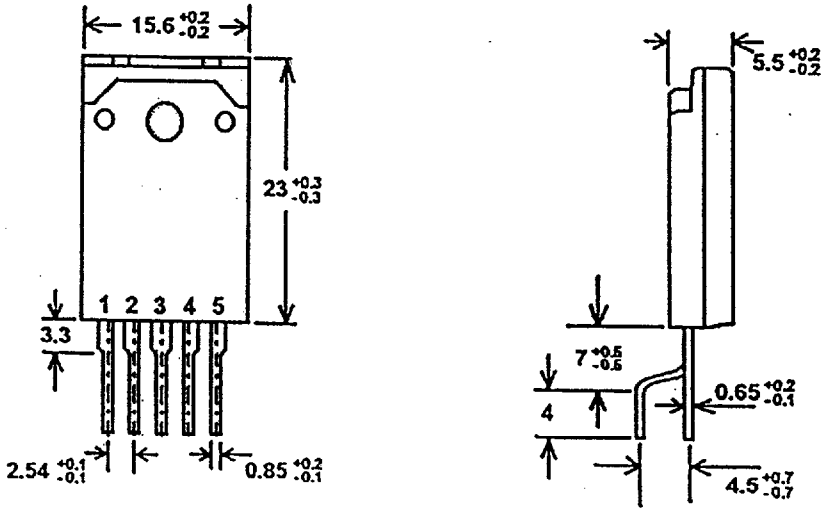
STR-F6600 Internal Circuit



Electrical Characteristics (refer to product specification for full details)

Absolute Maximum Ratings (Ta = 25°C)

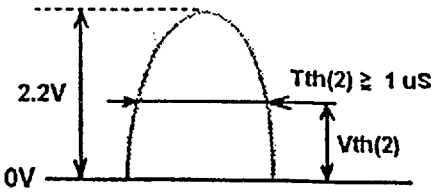
Parameter	Terminal	Symbol	Ratings	Unit	Note
Drain Current	3 - 2	Id peak	See individual specs	A	Single pulse
Maximum Switching Current	3 - 2	Id max	See individual specs	A	Vs-g = 0 - 0.78V Ta = -20 ~ +125°C
Single pulse avalanche energy	3 - 2	Eas	See individual specs	mJ	Single pulse
Input voltage for control circuit	4 - 5	Vin	35	V	
OCP/FB terminal voltage	1 - 5	Vth	6.0	V	
Power dissipation for MOSFET	3 - 2	Pd1	See individual specs	W	
Power dissipation for control circuit	4 - 5	Pd2	0.8	W	
Internal frame temperature in operation	----	Tf	-20 ~ +125	°C	
Operating ambient temperature	----	Top	-20 ~ +125	°C	
Storage temperature	----	Tstg	-40 ~ +125	°C	
MOSFET junction temperature	----	Tch	150	°C	



STR-F6600 Series - Outline Drawing

Recommended operating conditions

1. Inner frame temperature in operation Tf = 115°C maximum.
2. Time for input of quasi resonant signals.
   For the quasi resonant signal inputted to $V_{OCP/FB}$ terminal at the time of quasi resonant operation, the signal shall be wider than Tth(2).



Electrical Characteristics for Control Circuit

Vin = 18V (Ta = 25°C) unless otherwise specified.

Parameter	Terminal	Symbol	Ratings			Unit
			Min.	Typ.	Max.	
Operation start Voltage	4 - 5	Vin(on)	14.4	16	17.6	V
Operation stop voltage	4 - 5	Vin(off)	9	10	11	V
Operating circuit current	4 - 5	Iin(on)	—	—	30	mA
Circuit current, non-operational	4 - 5	Iin(off)	—	—	100	uA
Maximum OFF time	—	Toff(max)	45	—	55	usec
Minimum time for input of quasi resonant signals	1 - 5	Tth(2)	—	—	1.0	usec
Minimum OFF time	—	Toff(min)	—	—	1.5	usec
OCP/FB terminal threshold voltage 1	1 - 5	Vth(1)	0.68	0.73	0.78	V
OCP/FB terminal threshold voltage 2	1 - 5	Vth(2)	1.3	1.45	1.6	V
OVP operation voltage	4 - 5	Vin(ovp)	20.5	22.5	24.5	V
Latch circuit sustaining voltage	4 - 5	Iin(H)	—	—	400	uA
Latch circuit release voltage	4 - 5	Vin(La.off)	6.6	—	8.4	V
Thermal shutdown operating temperature	—	Tj(TSD)	140	—	—	°C

Lineup of STR-F6600 Series *

Type	MOSFET Vdss[V]	MOSFET Rds(on)Max	Vin [V] (a.c.)	Pout [W] ** [for guidance]
*** STR-F6612	400	1.65 ohm	100	58
STR-F6614	400	0.75 ohm	100	115
STR-F6616	400	0.42 ohm	100	190
*** STR-F6622	450	2.18 ohm	100	44
			120	60
*** STR-F6624	450	1.0 ohm	100	90
			120	120
*** STR-F6626	450	0.58 ohm	100	145
			120	190
*** STR-F6628	450	0.34 ohm	100	230
			120	290
*** STR-F6652	650	2.95 ohm	90 - 265	40
			220	86
STR-F6653	650	2.0 ohm	90 - 265	58
			220	120
STR-F6654	650	1.2 ohm	90 - 265	92
			220	190
*** STR-F6656	650	0.7 ohm	90 - 265	150
			220	300

* For details of MOSFET ratings see relevant device specifications.
** Absolute maximum output power can be 20 - 30% higher.
*** Samples available only.

Application Review

The STR-F6600 series is a range of integrated hybrid switch mode power regulators, combining in the same package a dedicated fully protected control IC together with a choice of avalanche rated rugged power MOS-FET; allowing the device to be tailored to the input voltage and power handling required. It is all housed in an isolated overmoulded SIP package eliminating the need for insulating components.

There are three possible modes of operation :

- Quasi Resonant (Demag sensing) flyback 20 - 300 KHz
  - Optimum EMI and efficiency
- Constant OFF time flyback (50uS fixed dead time) Pulse Ratio Control
  - Low power standby mode.
- Flyback operation synchronised to an external clock

Switching frequency is up to 300kHz

Voltage regulation is by peak current mode control and there is a genuine cycle by cycle current limit with no need for blanking.

Protection features include an Undervoltage Lockout with hysteresis to guard against over dissipation. Thermal protection is included.

The power limit can be controlled in an overload condition, reducing rectifier and MOSFET stresses regardless of input voltage. This is particularly important on start up to control the MOSFET losses and voltage stress.

STR-F6600 Family Functional Description & User Notes

Functions of each terminal and description of operation

Vin terminal (Pin 4): Start-up operation

The voltage on the Vin terminal (pin4) controls start-up and shutdown of the F6600.

Figure.1 shows a typical start up configuration. The Vin terminal voltage is shown in Fig.2

At start-up, C2 is charged through the start-up resistor Rs. When the Vin terminal voltage reaches 16V (typical), the control circuit enables regulator operation. Once the regulator starts, it draws 20mA nom. from C2 causing the voltage on C2 to fall momentarily. Once the regulator output voltage is established, the drive winding D starts to charge C2 via D2. The voltage on C2 thus recovers to the nominal drive voltage.

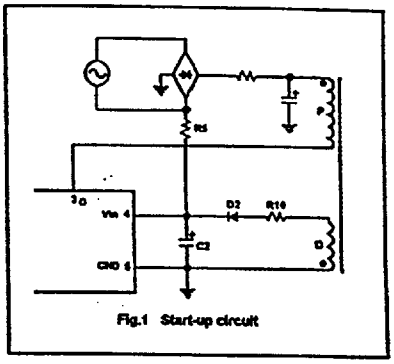


Fig.1 Start-up circuit

Value of Rs

As shown in Fig.3, the F6600 current is below 100uA max. (Tc=25°C) prior to Control circuit turn on. The latch circuit sustaining current is 400uA max. Thus 500uA (min.) should be allowed for in Rs at the lowest AC input voltage.

The value of Rs determines the charge time of C2 and thus the start up delay.

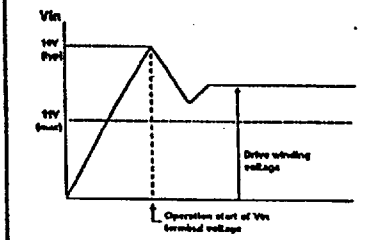


Fig.2 Waveform of Vin terminal voltage at start-up.

Value of C2

The choice of C2 is a trade off between an acceptable start up delay (in conjunction with Rs) and a hold up time sufficient to keep pin4 above its undervoltage shutdown threshold of 11V whilst the drive winding voltage is established. Typically C2 is in the range of 47-100uF for an acceptable hold up.

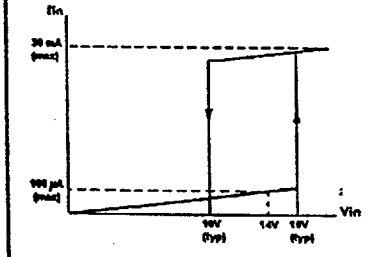


Fig.3 Vin terminal voltage circuit current Iin

Drive winding D

The turns ratio of the drive winding must be set such that in normal operation the voltage on C2 is above the shutdown voltage [Vin(off) 11V(max)] and below the OVP operating voltage [Vin(OVP) 20.5V(min)].

In the applications where there is a significant variation in Load current, the voltage on Vin may vary, as shown in Fig.4. This is due to peak charging of C2 In this case, adding a resistor R10 in the range a few ohms to tens of ohms in series with the rectifier diode D2 will bring the voltage variation within limits. The optimum resistance value of R10 should be determined using the actual transformer, since the voltage variation varies as a function of the coupling and so depends on transformer construction.

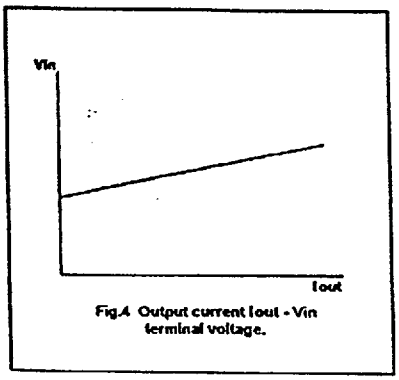


Fig.4 Output current Iout - Vin terminal voltage.

OCP/E.B (Pin 1): Constant Off Time, Quasi Resonant & Voltage Regulation Functions.

(Refer to Regulator Block Diagram [front page] and the Standard Application diagram [next page]) The internal oscillator uses the charge/discharge of an internal 4700pF capacitor (C1) to generate MOSFET drive signals. The

regulator has two modes of operation:

1. Fixed 50us off-time (Pulse Ratio Control mode)
2. Demagnetisation sensing (Quasi Resonant mode)

In both cases voltage regulation is achieved by mixing the opto-coupled voltage error and ramp proportional to drain current (Current Mode Control) and comparing this to an internal 0.73V reference. The comparator (OCP/FB comp) output pre terminates the oscillator. Which turns OFF the MOSFET drive signal.

The MOSFET is turned ON again when either the 4700 pF capacitor C1 discharges or a valid Quasi-Resonant signal is detected on Pin1.

Fixed 50us Off-Time: Pulse Ratio Control (PRC) Mode

This mode is the normal mode of operation in the absence of a Quasi-Resonant signal on Pin 1.

This can occur at start up and in overload and also can be commanded externally to provide low power Standby operation. This mode is inherently low dissipation and limits stresses/losses in the aforementioned conditions.

PRC Operation In Absence Of Feedback (Refer To Figure 6)

In the absence of a feedback signal (such as at the beginning of start up or if feedback is lost) the Drain current ramp, sensed across R5 and noise filtered by R4/C5 appears on Pin 1. When the ramp voltage on C5 exceeds the 0.73V reference signal, the comparator (OCP/FB comp) changes state, shutting down the oscillator and thereby turning OFF the MOSFET. Thus the voltage on the internal 4700 pF capacitor C1 is held high (6.5V) by the comparator (OCP/FB comp). When the comparator changes state, C1 now discharges via the Off-Time Resistor; the voltage on C1 ramps down and when it reaches 3.7V, the oscillator turns ON the

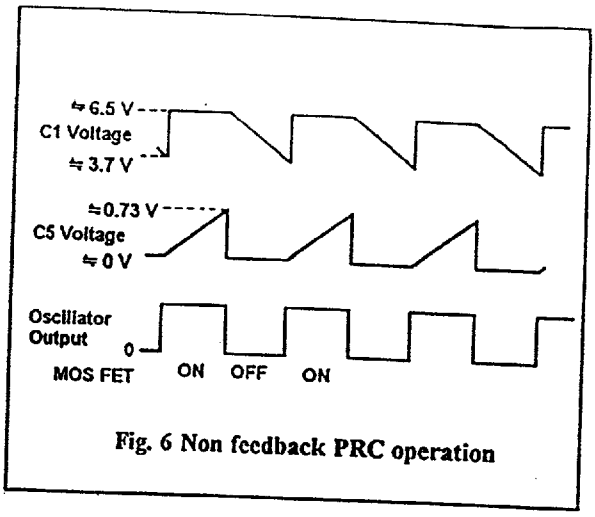


Fig. 6 Non feedback PRC operation

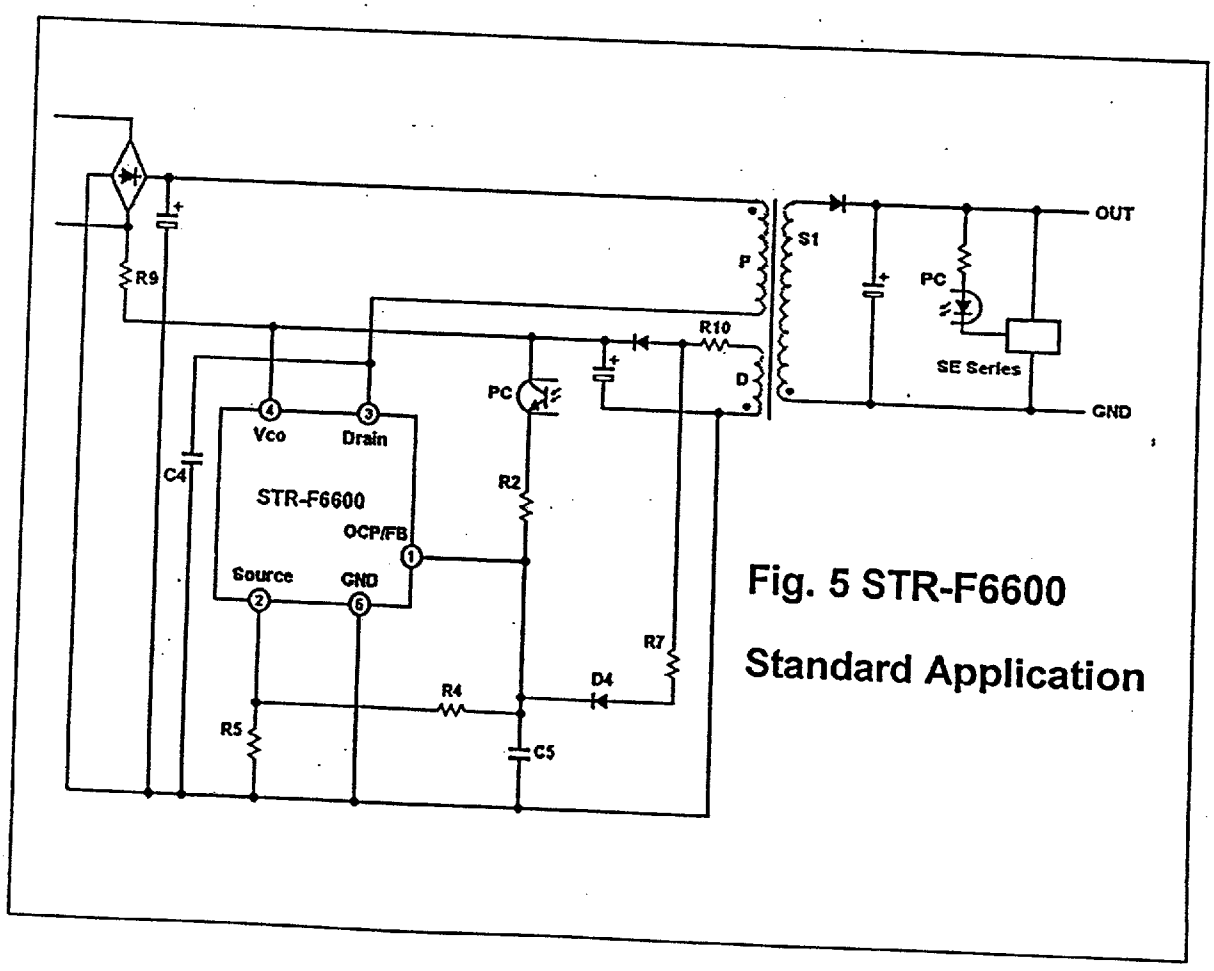


Fig. 5 STR-F6600

Standard Application

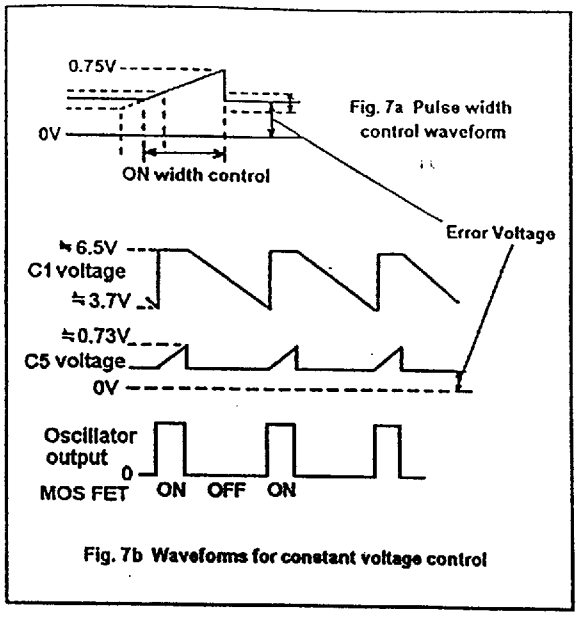


Fig. 7a Pulse width control waveform

Fig. 7b Waveforms for constant voltage control

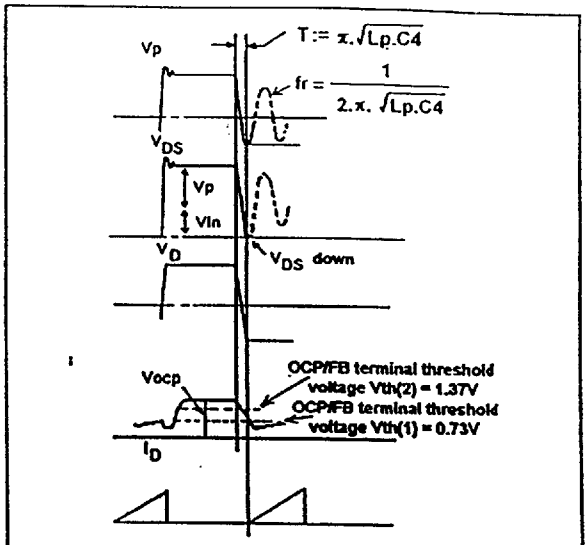


Fig. 8 Waveform of each section.

MOSFET. This ramp-down time is internally trimmed to 50us. The comparator (OCP/FB comp) changes state again and so the cycle repeats. So, in the absence of feedback, the maximum current in the MOSFET and thereby the maximum stresses and load power can be controlled by the value of R5.

R5 can be selected such that

$R5 <= ID_{LIMIT}/0.73V$

(also see par. on Over Current Protection)

PRC Operation With Voltage Feedback (Refer To Figure 7a & Figure 7b)

Output voltage control is achieved by the opto-coupled feedback current (proportional to the output Voltage error signal) across resistor R4 and summing this with the Drain current ramp on R5. The signal on pin1 is therefore the composite of the Output Voltage error signal and the drain current ramp. The DC bias signal across R4 is thus a function of the load

Consequently at light load the bias signal on R4 is closer to the threshold voltage of the comparator (OCP/FB comp).

To eliminate the possibility of false shutdown at MOSFET Turn ON (when there is a current spike due to the discharge of primary capacitance), a constant current sink of 1.35 mA is turned on, effectively lowering the input impedance on pin1, this effectively momentarily increases the shutdown threshold.

Demagnetisation sensing (Quasi Resonant) mode

(Refer to Regulator Block Diagram [front page] and Standard Application diagram [back one page] & Figure 7a)

Voltage control is performed as described above for PRC mode but instead of having a fixed dead time, the demagnetisation of the transformer is sensed (that is, no O/P current flowing) by a second comparator (INH comp) with a threshold of 1.37V.

The rising edge of the Q/R signal, VOCP resets the oscillator after a fixed delay so that the falling edge of the Q/R signal VOCP changes the state of the OCP/FB comparator at 0.73V, turning on the MOSFET.

Since ON time reduces with increasing line voltage and OFF time with increasing load, it follows that in Q/R operation the minimum switching frequency, fmin, is at minimum line & maximum load. Conversely the maximum switching frequency, fmax., is at maximum line & minimum load.

The F6600 series can operate in Q/R flyback mode at frequencies up to 300kHz.

Q/R Sensing and Delay

Q/R sensing makes use of the natural magnetising & leakage inductances and self capacitances associated with the Flyback power stage.

Figure 8 shows the Drain voltage waveform, VDS, (Pin3 of the F6600) as well as VP, the voltage on the primary of the transformer.

Once the current in the output diode stops flowing, the primary stored energy 'rings' as shown on VP & VDS. This is the so called 'Ringing Choke'.

The resonant frequency is given by the magnetising inductance of the transformer and the capacitor C4.

The addition of this capacitor fixes the ringing frequency and reduces the harmonic content in the VDS waveform, lowering EMI. Also since VDS falls to zero during the first half cycle of the ring this point can be sensed and used to turn on the MOSFET with no voltage across it. Thus the MOSFET is Zero Voltage and Zero Current switched (ZVS/ZCS).

The voltage VOCP(Pin1) follows the form of the VDS

waveform. The condition for Q/R operation is as follows:

2.0V <VOCP> 5.5V for > 1us. (Also See Section2)

With R4 = 680 ohm and current source of 1.35mA then for a value of Vocp in the range +2V to +5.5V the effective impedance on Pin 1 (R_{EFF}) is given by :

$$R_{EFF} = (680 \cdot Vocp)/(Vocp + 0.918)$$

Thus for Q/R operation the value of R7 is given by :

$$R7 = \frac{680\,(V_D - V_{(D4)} - Vocp)}{Vocp + 0.918}$$

Where : V_D is the voltage on the drive winding and $V_{(D4)}$ is the forward voltage bdrop on D4.

Transformer Primary Inductance Calculation

Transformer design is exactly as for any other RCC type Flyback, except that the value of Primary Inductance, Lp, must take into account the Q/R delay time T (See Figure 8) Since this affects the duty cycle D.

Lp is given by:

$$Lp = \frac{(Vinmin.Dmax)^2}{(\sqrt{((2.Po.fmin)/\varepsilon)} + Vinmin.\pi.fmin.dmax.\sqrt{C4})^2}$$

Where

Po = Maximum. O/P Power

fmin = Minimum Switching Frequency.

ε = Regulator Efficiency

Dmax = Duty Cycle at fmin

VINmin = VDC on Electrocap C1 at VACMin.

Thus the resonant frequency; fr, of the Q/R power cell is given by

$$fr = \frac{1}{2\pi.\sqrt{(Lp.C4)}}$$

For optimum EMI/efficiency performance, Q/R turn off is achieved when the MOSFET is ZVS & ZCS; that is at one half cycle of the Q/R frequency; fr.

This is given by time T as follows:

$$T := \pi.\sqrt{(Lp.C4)}$$

OCP/FB (Pin 1): Over Current Protection (OCP) Functions

(Refer to Regulator Block Diagram [front page] and Standard Application diagram [back two pages])

The regulator implements pulse-by-pulse overcurrent protection which limits the maximum drain current in the MOSFET on every pulse by switching off the internal drive to the MOSFET.

The oscillator output. Fig.7 shows the overcurrent detection circuit. The MOSFET drain current is detected by inputting the voltage drop of R5 connected between the Source terminal (Pin 2) of the MOSFET and the GND terminal (Pin 5) into the OCP/FB terminal (Pin 1).

This action is exactly the same by which normal current mode control is achieved.

Drive circuit

(Refer to Regulator Block Diagram on front page)

This circuit is driven from the oscillator and provides the current drive to charge and discharge the MOSFET Gate-source capacitance, thereby turning the device On & OFF. .

As shown in the Regulator Block Diagram, the basic circuit configuration is totem-pole type with an additional limiting resistor in the gate circuit at turn ON. This limits the turn on speed of the MOSFET, thereby reducing EMI due to the discharge of primary capacitance.

This is possible because of the ZVS/ZCS nature of the turn ON (See earlier par.)

The turn OFF resistor is lower, allowing the device turn OFF current to be increased. This reduces the turn OFF loss in the MOSFET

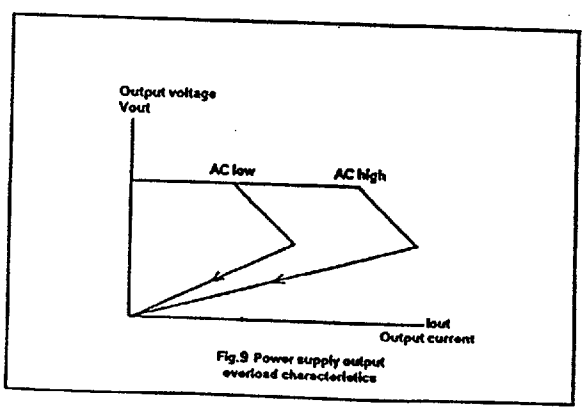


Fig.9 Power supply output overload characteristics

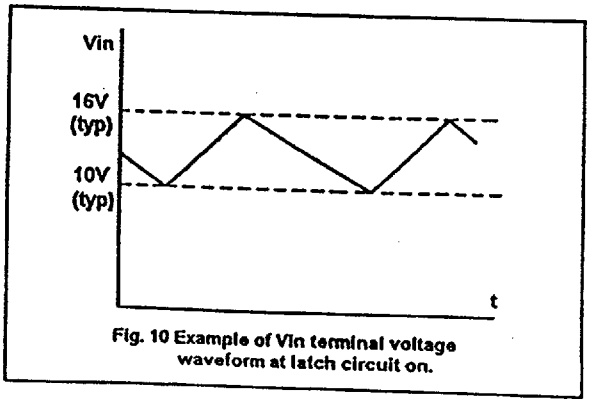


Fig. 10 Example of Vin terminal voltage waveform at latch circuit on.

The gate drive Voltage (8.3V) is such that even with 0.73V across R5 (Drain Current sense resistor), the MOSFET is fully enhanced, allowing full use to be made of its high current handling capacity.

Latch Circuit

The latch circuit keeps the oscillator output low to inhibit operation of the regulator when overvoltage protection(OVP) and thermal shutdown (TSD) circuits are in operation. As long as the latch hold-in current is 400uA (max.) (supplied via Rs) with Vin at 8.5V(Pin4), the regulator will stay in the OFF state

An internal capacitor provides a 10us delay to prevent spurious shutdown.

With the latch 'ON', the voltage on Pin 4 cycles between 16V and 10V as shown in Figure 10. This is due to the higher current drawn when the Pin4 is at 16V compared to that drawn close to shutdown (10V).

Pulling Vin (Pin4) below 6.5V will reset the latch circuit, re-enabling the regulator.

Thermal shutdown

This internal facility triggers the latch if the frame temperature of the regulator exceeds 140°C (typ.).

The temperature is sensed on the control IC, but also protects against overheating of the MOSFET as the MOSFET and the control IC are mounted on the same lead frame.

Over voltage protection circuit

The F6600 sets the latch circuit when the Vin voltage (Pin4) exceeds 22.5V(typ.). Since the voltage on Pin4 is proportional to the output voltage through the transformer turns ratio, the regulator protects the output against Overvoltage. This function is entirely independent of the Output Voltage regulation loop and indeed will protect against output overvoltage should the Voltage Error signal be lost. The measure of overvoltage is given by:

$$VoutOVP = \frac{(VoutNOMINAL . VinOVP)}{VinNOMINAL}$$

Where: VinOVP is the Drive Voltage on Pin4.

So in an overvoltage sensitive application, the Drive voltage can be set to close to 20V and thus will protect the output, if it rises more than 10% above nominal.

Component Selection.

Capacitors

Electrolytic capacitors carrying large Switching Frequency ripple currents (C1 and O/P capacitors) should be selected to handle the high ripple. currents involved. (These are calculated by the Transformer Design Spreadsheet). Capacitor with low ESR (SMPS standard) are suitable.

The Q/R capacitor C4 should be a High Voltage ceramic or polypropylene with low ESR suitable for pulsed current operation.

The safety critical nature of the off-line application must be considered when selecting both X & Y capacitors for common and differential mode noise filtering. Use of the low noise Q/R F6600 may reduce these capacitor values.

C5, the 470pF filtering cap should be a 50V COG dielectric ceramic type or any good HF capacitor with a withstanding voltage of >10V.

Resistors

Resistor R5 carries high frequency current, and so a low inductance type capable of handling the power dissipation rating should be used.

Resistor R9 (Rs) should be capable of handling the power and voltage ratings.

Diodes.

Diodes carrying the high frequency flyback currents such as the transformer rectifier diodes should have a fast/ultrafast reverse recovery characteristic, sifficient current handling and PIV rating. The Transformer Design Spreadsheet details diode current rating & PIV. Allegro SanKen supplies a range of suitable diodes, and these are detailed in the Allegro SanKen Short-form Catalogue.

Transformer.

The choice of the transformer is greatly facilitated by using the Transformer Design Spreadsheet and the Q/R Power Cell Operating Frequency Selection Tool.

Because of high frequency effects, it is recommended to use multifilar, small diameter wire.

Opto-coupler

Both TLP 621 and Siemens SFH 610A2/615A2 are suitable. A CTR range of 50-200% is acceptable.

Error Amplifier

A standard TL 431 programmable shunt regulator or an Allegro-SanKen SE series Error Amplifier can be used. The SE series is particularly well suited to High Voltage (70-140V) O/P's, as the TC of the divider chain is matched. There are SE series error amplifiers in the range 5V to 140V.

If an Allegro-Sanken (SE series) error amplifier is used, normally phase compensation is not required. Should additional high frequency attenuation be required a capacitor C6 (0.1uF or less) can be connected across the primary side (Collector-Emitter) of the opto-coupler, a diode D6 should be included to prevent changing the Q/R timing.

Application Support

Note: The following design tools and publications are available to support applications for STR F6600 as well as other Allegro SanKen Q/R Flyback Regulators These allow easy power cell assessment and design, leading to rapid, straightforward circuit implementation.

- MathCad Q/R Power Cell Operating Frequency Selection Tool.
- Prototyping PCB (PSA 50015AH)
- Sample Schematic 30W: 90-265V I/P (Uses PSA50015AH PCB) ***
- Sample Schematic 100W: 170-265V (Uses PSA50015AH PCB) ***
- Users Guide to STR F6600. Tips & Techniques for Optimum Regulator Performance. (available soon)
- All You Ever Wanted To Know About Switched Mode Power Systems (Introduction to Switched Mode Power Conversion In General & The Allegro-SanKen Q/R Flyback Approach In Particular)

To obtain any of the above: Contact your local Allegro-Sanken Representative or Distributor. Alternatively contact Allegro-Sanken direct at :

Allegro MicroSystems Europe Ltd., Balfour House, Churchfield Road, Walton-on-Thames, Surrey, KT12 2TD, United Kingdom.

Tel: 44 1932 253355 Fax: 44 1932 246622

Allegro MicroSystems Europe Ltd., (Bureau De Liason), 27 Rue De La Paix, F-74000 Annecy, France

Tel : 33 45051 2359 Fax : 33 45051 2083

Allegro Microsystems Inc., 115 Northeast Cutoff, Box 15036, Worcester, MA 01615, USA.

Tel : 1 508 853 5000 Fax : 1 508 853 7861

Sanken Electric Company Ltd., 1-11-1 Nishi-Ikebukuro, Toshima-ku, Tokyo, Japan.

Tel : 81 3 3986 6164 Fax : 81 3 3986 1400

Sanken Electric Company Ltd., Lotte Bldg. (22nd Floor), 1 Sokong-dong, Chung-ku, Seoul, Korea.

Trl : 82 2 776 4206 Fax : 82 2 757 3248

Allegro/Sanken does not assume any liability arising from the use of any device or circuit described herein.

*** These allow understanding of Q/R operation techniques. The customer should apply their own layout rules; particularly with respect to EMC and voltage clearances.

Lineup of STR−F6600 series

(direct feedback quasi resonant switching regulator)

03 April 1998

Type#2 [replaced model]#3	MOSFET VDSS[V] RDS(on)MAX.	VIN[V]	Pout [W]	engineering sample	mass production
STR-F6612 [STR-F6502]	400 1.58 Ω	100	60	end Apr.,'98	end Aug.,'98
STR-F6614 [STR-F6511]	400 0.76 Ω	100	115	OK	in production
STR-F6616 [STR-F6513]	400 0.42 Ω	100	190	OK	in production
STR-F6624 [STR-F6514]	450 0.92 Ω	100	98	OK	in production
		120	130		
STR-F6626 [STR-F6516]	450 0.58 Ω	100	145	OK	in production
		120	190		
STR-F6628	450 0.35 Ω	100	225	OK	in production
		120	290		
STR-F6632	500 2.62 Ω#1	100	36	end Apr.,'98	not yet fixed
		120	50		
STR-F6652	650 2.8 Ω	WIDE	40	OK	in production
		220	86		
STR-F6653 [STR-F6523]	650 1.95 Ω	WIDE	58	OK	in production
		220	120		
STR-F6654 [STR-F6524]	650 1.15 Ω	WIDE	92	OK	in production
		220	190		
STR-F6656	650 0.71 Ω	WIDE	150	OK	in production
		220	300		
STR-F6672 [STR-F6535]	900 7.7 Ω	220	25(no fin)	OK	not yet fixed
			50		
STR-F6674	900 4.49 Ω#1	WIDE	28	end Apr.,'98	not yet fixed
		220	76		
STR-F6676 [STR-F6537]	900 2.81 Ω	WIDE	44	OK	in production
		220	115		

Notes:#1.RDS values are objective ones , as the MOSFET is under development.

#2.Type names are provisional.

#3.[ ]shows equivalent F6500series.