AN5163K

NTSC Color-TV Signal Processor IC

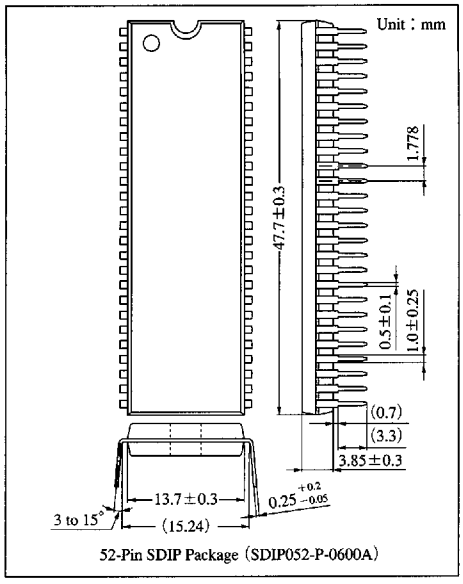
■ Overview

The AN5163K is a single-chip IC which incorporates all functions needed for NTSC color-TV signal processing.

And sets production line will be rationalized by built-in I²C bus interface.

■ Features

- Built-in VIF, SIF, video signal processing, chroma signal processing, and synchronization signal processing circuits
- Built-in an I²C bus interface circuit

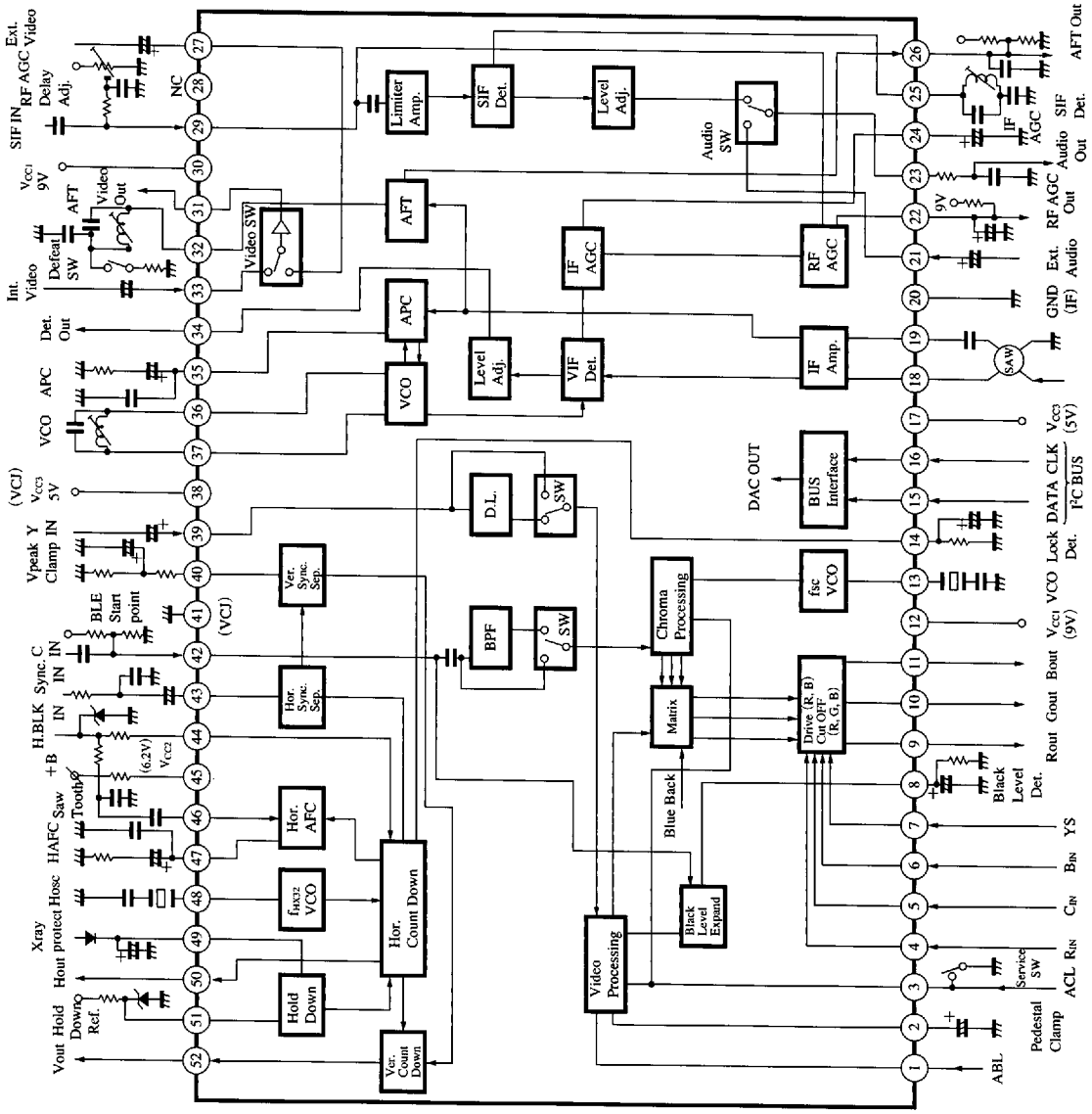


52-Pin SDIP Package (SDIP052-P-0600A)

■ Pin Descriptions

Pin No.	Pin name	Pin No.	Pin name
1	ABL/Neck protection	27	EXT.Video input
2	Pedestal clamp	28	NC
3	ACL/Service switch	29	SIF In/RF AGC delay
4	R input	30	V_{CC1} (2) VIF/SIF system
5	G input	31	Video output
6	B input	32	AFT coil
7	YS input	33	Int.Video input
8	Black Det. /Blank off/Sub Color	34	VIF detection output
9	R output	35	APC (VIF)
10	G output	36	VCO coil (1)
11	B output	37	VCO coil (2)
12	V_{CC1} (1) video/chroma system	38	V_{CC3} (1) video/jungle system
13	Chroma VCO	39	Y input
14	Lock detection	40	Ver. peak clamp
15	SDA	41	GND (1) video/chroma/jungle system
16	SCL	42	Chroma In/Black Level Start
17	V_{CC3} (2) VIF/SIF system	43	Sync. input
18	VIF input (1)	44	FBP input
19	VIF input (2)	45	V_{CC2} jungle system
20	GND (1) VIF/SIF system	46	Saw Tooth
21	Ext. Audio input	47	Hor. AFC
22	RF AGC output	48	Hor. OSC
23	Audio output	49	X-ray protection
24	IF AGC	50	Hor. output
25	SIF detection	51	Hold Down Ref.
26	AFT output	52	Ver. output

Block Diagram



■ Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit
Supply voltage	V_{CC}	$V_{CC1(12,30)}$	10.5	V
		$V_{CC3(17,38)}$	6.0	
Supply current	I_{CC}	I_{12+30}	78	mA
		I_{17+38}	86	
		I_{45}	27	
Power dissipation Note 2)	P_D	1,480		mW
Operating ambient temperature Note 1)	T_{opr}	−20 to +70		℃
Storage temperature Note 1)	T_{stg}	−55 to +150		℃

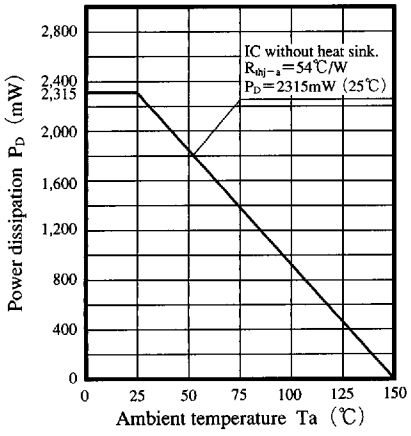
Note 1) Ta=25℃ except operating ambient temperature and storage temperature.
Note 2) Allowable power dissipation of the package at Ta=70℃.

■ Recommended Operating Range (Ta=25℃)

Parameter	Symbol	Range
Operating supply voltage range	V_{CC1}	8.1V to 9.9V
	V_{CC3}	4.5V to 5.5V
Operating supply current range	I_{45}	10mA to 25mA

■ Reference

$P_D - Ta$



■ Electrical Characteristics (Ta=25±2℃)

Parameter	Symbol	Condition	min	typ	max	Unit
Supply current (1)	I_{30}	Current when V_{30}=9V	6	10	12	mA
Supply current (2)	I_{17}	Current when V_{17}=5V	22	28	34	mA
Supply current (3)	I_{12}	Current when V_{12}=9V	38	49	60	mA
Supply current (4)	I_{38}	Current when V_{38}=5V	26	33	40	mA
Stabilized supply current	I_{45}	Current when V_{45}=5V	3	5	7	mA
Stabilized supply voltage	V_{45}	V_{45} when I_{45}=15mA	5.6	6.3	6.9	V
Video SW input terminal voltage	$V_{27,33}$		2.2	2.6	3.0	V
External input terminal voltage	V_{21}	DC measurement	3.5	4.0	4.5	V
Synchronous separation input clamp voltage	V_{CL}		1.2	1.5	1.8	V
Output resistor (Pin㉞)	R_{o34}	DC measurement	20	60	150	Ω
Input resistor (Pin㉗, ㉝)	$R_{i\,27,33}$	DC measurement	27	37	47	kΩ
Output resistor (Pin㉛)	R_{o31}	DC measurement	20	60	150	Ω
Output resistor (Pin㉓)	R_{o23}	DC measurement	200	400	600	Ω
Input resistor (Pin㉑)	$R_{i\,21}$	DC measurement	55	65	75	kΩ
VIF Circuit		(The test condition for below is f_P=45.75MHz Vin=90dBμ)				
Video detection output (typ.)	V_{o34}	m=87.5% DATA 0B=8 (typ.)	1.3	1.6	1.9	V_{P-P}
Video detection output (max.)	$V_{o34max.}$	DATA 0B=F, ratio to typ.	1.3	2.3	4.0	dB
Video detection output (min.)	$V_{o34min.}$	DATA 0B=0, ratio to typ.	−6.0	−3.0	−1.5	dB
Video detection output f characteristics	f_{pc}	Frequency of output −3dB for 1MHz	5.5	8	11	MHz
Synchronous peak value voltage	V_{sp}	m=87.5% DATA 0B=8	1.7	2.1	2.5	V
Video detection output DC voltage	V_{34}	No input IF AGC min.	3.3	3.9	4.5	V
APC pull-in range (H)	f_{pph}	Pull-in range of high band side	0.6	1.3	—	MHz
APC pull-in range (L)	f_{ppl}	Pull-in range of low band side	—	−1.3	−0.6	MHz
VCO control sensitivity	β_P	ΔV_{35}=0.2V	1.3	2.2	3.1	kHz/mV
RF AGC sensitivity	G_{RF}	Input level difference to become V_{22}=1V→7V	—	3.0	4.5	dB
RF AGC maximum voltage	$V_{22max.}$		8.9	9.0	9.1	V
RF AGC minimum voltage	$V_{22min.}$		0	0.2	0.5	V
AFT discrimination sensitivity	μ_{AFT}	Δf=±25kHz	18	29	40	mV/kHz
AFT center voltage	V_{26C}	Vin no input	3.6	4.8	6.0	V
AFT maximum output voltage	$V_{26max.}$	$f=f_p-500kHz$	7.3	7.8	8.3	V
AFT minimum output voltage	$V_{26min.}$	$f=f_p+500kHz$	0	0.6	1.0	V
AFT detection terminal voltage	V_{32}		2.3	2.8	3.3	V
Video SW voltage gain	G_{VSW}	f=1MHz Vin=$1V_{P-P}$	3.0	4.6	6.0	dB
Video SW f characteristics	f_{VSW}	At −3dB from f=1MHz Vin=$1V_{P-P}$	8.5	12	—	MHz
Sound IF output	V_{SIF}	V_p=90dBμ V_s=70dBμ	94	100	106	dBμ
Video SW output difference voltage	ΔV_{VSW}		−0.5	0	0.5	V
SIF Circuit		(The test condition for below is f_S=4.5MHz Vin=90dBμ)				
Audio detection output (standard)	Vo_{23}	Δf=±25kHz fm=400Hz DATA 0C=8 (typ.) R_D=4.7kΩ	350	450	550	mVrms
Audio detection output (min.)	$Vo_{23max.}$	DATA 0C=F, ratio to typ.	2	2.8	4.5	dB
Audio detection output (max.)	$Vo_{23min.}$	DATA 0C=0, ratio to typ.	−9	−5	−2	dB
Audio output DC voltage (Ext.)	V_{23EX}	DATA 0D−1=1 (external)	3.5	4.0	4.5	V
Audio SW voltage gain	G_{ASW}	DATA 0D−1=1 (external)	−3	−1	+1	dB

■ Electrical Characteristics (cont.) (Ta=25±2℃)

Parameter	Symbol	Condition	min	typ	max	Unit
Video Signal Processing Circuit	(The test condition for below is established to be input 0.7V_{P-P} stair step wave Gout)					
Video output (standard)	V_{YO}	DATA 03=41 (typ.) (contrast)	1.8	2.4	3.0	V_{P-P}
Video output (max.)	$V_{YOmax.}$	DATA 03=7F (max.)	3.3	4.3	5.3	V_{P-P}
Video output (min.)	$V_{YOmin.}$	DATA 03=00 (min.)	0.3	0.5	0.7	V_{P-P}
Contrast variable range	$YC_{max./min.}$	$\frac{03=7F}{03=00}$	15.0	19.0	23.0	dB
Video frequency characteristics	f_{YC}	DATA 04=00 (sharpness) at −3dB	6.0	7.5	—	MHz
Sharpness variable range	$YS_{max./min.}$	$\frac{04=7F}{04=00}$	7.0	10.5	14.0	dB
Pedestal level (standard)	V_{ped}	DATA 02=81 (typ.) (brightness)	1.8	2.4	3.0	V
Pedestal variable range	ΔV_{ped}	Difference between DATA 02=00 and FF	1.7	2.2	2.7	V
Brightness control sensitivity	ΔV_{BRT}	Variation range of DATA 02=60 to A0	8.0	11.0	14.0	mV/bit
Video input clamp voltage	V_{39}		3.2	3.7	4.2	V
ACL sensitivity	ACL		2.0	2.6	3.3	V/V
ABL sensitivity	ABL		0.9	1.1	1.3	V/V
Blanking level	V_{YBL}	DC voltage of blanking pulse	0.5	1.0	1.5	V
DC restoration rate	T_{DC}	APL10% to 90%	95	100	105	%
Service SW threshold voltage	V_{SSW}		0.3	0.5	0.9	V
Neck protector threshold voltage	V_{NP}		0.3	0.5	0.9	V
Blanking OFF threshold voltage	V_{BOFF}		0.3	0.5	0.9	V
Color Signal Processing Circuit	(The test condition for below is burst 150mV_{P-P}, where B out as reference)					
Color difference output (standard)	VCO	Input : color bar DATA 00=41 (typ.)	1.4	1.9	2.4	V_{P-P}
Color difference output (max.)	$VCO_{max.}$	DATA 00=7F, amplitude on one side	2.5	3.2	3.9	V_{O-P}
Color difference output (min.)	$VCO_{min.}$	DATA 00=00	—	0	100	mV_{P-P}
Contrast variable range	$CC_{max./min.}$	$\frac{03=7F}{03=00}$	15	18	22	times
ACC characteristics (1)	ACC_1	Burst 150→300mV_{P-P}	0.9	1.0	1.2	times
ACC characteristics (2)	ACC_2	Burst 150→30mV_{P-P}	0.7	1.0	1.1	times
Tint center	$\Delta\theta_C$	Difference from DATA 01=41 (tint)	−13	0	+13	bit
Tint variable range (1)	$\Delta\theta_1$	DATA 01=7F	30	45	60	deg
Tint variable range (2)	$\Delta\theta_2$	DATA 01=00	−60	−45	−30	deg
Demodulation output ratio (R)	R/B		0.76	0.96	1.15	times
Demodulation output ratio (G)	G/B		0.27	0.34	0.41	times
Demodulation output angle (R)	∠R		92	104	116	deg
Demodulation output angle (G)	∠G		224	236	248	deg
Color killer tolerance	V_{Kill}	0dB=150mV_{P-P}, BPF OFF	−49	−39	−33	dB
APC pull-in range (H)	f_{CPH}		450	700	—	Hz
APC pull-in range (L)	f_{CPL}		—	−1000	−450	Hz
RGB Processing Circuit						
Pedestal difference voltage	ΔV_{IPL}	Difference voltage of RGB out pedestal	−0.3	0	0.3	V
Brightness voltage tracking	ΔT_{BL}	DATA 02 (bright) difference between 02=41 to C1	0.9	0	1.1	times

■ Electrical Characteristics (cont.) (Ta=25±2℃)

Parameter	Symbol	Condition	min	typ	max	Unit
Video voltage gain relative ratio	ΔG_{YC}	R,Bout output ratio to Gout	0.8	1.0	1.2	times
Video voltage gain tracking	ΔT_{cont}	DATA 03 (contrast), ratio of 03=21 to 61	0.9	1.0	1.1	times/ times
Drive adjustment range	G_{DV}		4.0	6.0	8.0	dB
Cut-off adjustment range	$V_{cut-OFF}$		1.9	2.2	2.5	V
Y_S threshold voltage	V_{YS}	Minimum level at which YS is ON	0.7	1.0	1.3	V
External RGB pedestal voltage	V_{EPL}		1.8	2.4	3.0	V
External RGB pedestal difference voltage	ΔV_{EPL}		−250	0	250	mV
Internal/external pedestal difference voltage	$\Delta V_{PL/IE}$	Internal-external	−250	0	250	mV
External RGB output voltage	V_{ERGB}		4.1	5.1	6.1	V_{P-P}
External RGB output difference voltage	ΔV_{ERGB}		−0.6	0	+0.6	V
External RGB contrast variable range	$EC_{max./min.}$		15	18	22	dB
Blue-back output voltage (1)	V_{BB1}	DATA 0D−0 (blue-back) Bout at 0D−0=0	2.5	3.5	4.5	V_{P-P}
Blue-back output voltage (2)	V_{BB2}	DATA 0D−0 (blue-back) R,Gout at 0D−0=0	−0.5	0	+0.5	V
Synchronizing Signal Processing Circuit						
Horizontal free-run oscillation frequency	f_{HO}		15.45	15.75	16.05	kHz
Horizontal output pulse duty	τ_{HO}		32	38	44	%
Horizontal pull-in range	f_{HP}		±500	±650	—	Hz
Vertical free-run oscillation frequency	f_{VO}		58	60	62	Hz
Vertical output pulse width	τ_{VO}	f_H=15.75kHz f_V=60Hz	0.57	0.64	0.71	ms
Vertical pull-in range	f_{VP}	f_H=15.75kHz	56	—	64	Hz
Vertical blanking pulse width	τ_{VB}	Measure at RGB out	0.9	1.1	1.3	ms
Horizontal output voltage (H)	V_{50H}		2.4	2.7	3.0	V
Horizontal output voltage (L)	V_{50L}		—	0	0.3	V
Vertical output voltage (H)	V_{52H}		4.0	4.3	4.6	V
Vertical output voltage (L)	V_{52L}		—	0	0.3	V
Picture center variable range	ΔT_{HC}		3.0	3.7	4.5	μs
I²C Interface						
Sink current at ACK time	I_{ACK}		2.0	2.5	—	mA
SCL, SDA signal input High Level	V_{HIGH}		3.1	—	—	V
SCL, SDA signal input Low Level	V_{LOW}		—	—	0.9	V
Input maximum frequency	$f_{imax.}$		100	—	—	kbit/s
VIF Circuit		(The test condition for below is f_P=45.75MHz)				
Input sensitivity	V_{PS}	Vo_{34}=−3dB	—	(46)	(52)	dBμ
Maximum input	$V_{Pmax.}$	Vo_{34}=+1dB	(103)	(106)	—	dBμ
SN ratio	S/N_P	Vin=90dBμ	(50)	(53)	—	dB
Differential gain	DG_P	Vin=90dBμ	(0)	(3)	(5)	%
Differential phase	DP_P	Vin=90dBμ	(0)	(3)	(5)	deg
Black noise detection level	ΔV_{BN}		(−0.95)	(−0.75)	(−0.55)	V
Black noise clamp level	ΔV_{BNC}		(0.28)	(0.48)	(0.68)	V
VCO switch ON drift	Δf_p	Oscillation frequency drift during 5 second to 5 minutes after sw. on	(−50)	(150)	(300)	kHz
Intermodulation	IM		(46)	(52)	—	dB
Input resistance (Pin⑱, ⑲)	$Ri_{18, 19}$	f=45.75MHz	(1.0)	(1.3)	(1.6)	kΩ
Input capacitance (Pin⑱, ⑲)	$Ci_{18, 19}$	f=45.75MHz	(3.2)	(4.0)	(4.8)	pF

■ Electrical Characteristics (cont.) (Ta=25±2℃)

Parameter	Symbol	Condition	min	typ	max	Unit
AFT defeat SW operation voltage	V_{AFTSW}	Maximum voltage at V_{26}=4.5±0.5V DC	(0.5)	(1.3)	(2.2)	V
Video SW crosstalk	CT_{VSW}	f=1MHz	—	(−70)	(−60)	dB
SIF Circuit						
Input limiting level	V_{Lim}	Vo_{23}=−3dB	—	(43)	(49)	dBμ
AM rejection ratio	AMR	AM=30% Vin=90dBμ	(45)	(55)	—	dB
Total harmonics distortion ratio	THD	Vin=90dBμ	(0)	(0.3)	(0.5)	%
Audio SW crosstalk	CT_{ASW}	Vin=90dBμ	—	(−96)	(−90)	dB
Video Signal Processing Circuit		(The test condition below is to be measured at G out)				
Delay line ON/OFF gain difference	ΔG_{DL}	Ratio of $\frac{\text{DL ON}}{\text{DL OFF}}$	(0.9)	(1.0)	(1.1)	times
Y signal delay time	T_{DL}	Phase difference between DATA 0D−4=0 (DL exists) and Y input (Pin㊴)	(390)	(460)	(530)	ns
Delay time drift	ΔT_{DL}	Phase difference between DATA 0D−4=0 and 0D−4=1	(200)	(240)	(280)	ns
Black level correction (1)	V_{BL1}	Input : full black, difference between black correction SW 9V and OPEN	(−100)	(0)	(100)	mV
Black level correction (2)	V_{BL2}	Input : full black, difference between black correction SW 3V and 9V	(400)	(700)	(1000)	mV
Black level correction (3)	V_{BL3}	Input:approx. 20IRE, voltage difference between black correction SW open and 9V	(100)	(300)	(500)	mV
Black level correction start point (1)	V_{BS1}	V_{42}=2.5V	(40)	(45)	(50)	IRE
Black level correction start point (2)	V_{BS2}	V_{42}=4.5V	(27)	(32)	(37)	IRE
Black level correction start point (3)	V_{BS3}	V_{42}=6.5V	(15)	(20)	(25)	IRE
Contrast variation with sharpness	ΔV_{CS}		(−300)	(0)	(+300)	mV
Brightness variation with sharpness	ΔV_{BS}		(−250)	(0)	(+250)	mV
Input dynamic range	V_{Imax}		(0.9)	(1.1)	—	V_{P-P}
Y signal SN ratio	S/N_Y		(53)	(59)	—	dB
Video output V_{CC} variation	$\Delta V_{Y/Vcc}$	V_{CC1}=8.1 to 9.9V	(0.0)	(0.1)	(0.25)	V_{P-P}/V
Pedestal level V_{CC} variation	$\Delta V_{PL/Vcc}$	V_{CC1}=8.1 to 9.9V	(0)	(150)	(300)	mV/V
Color Signal Processing Circuit		(The test condition below is burst 150mV_{P-P}, where reference Bout)				
Demodulation output residual carrier	V_{car}		—	(20)	(50)	mV_{P-P}
BPF frequency characteristics (1)	f_{BPF1}	BPF exists. $\frac{\text{f=4MHz}}{\text{f=3.58MHz}}$	—	(3)	—	dB
BPF frequency characteristics (2)	f_{BPF2}	BPF exists. $\frac{\text{f=3MHz}}{\text{f=3.58MHz}}$	—	(−6)	—	dB
BPF frequency characteristics (3)	f_{BPF3}	BPF exists. $\frac{\text{f=2MHz}}{\text{f=3.58MHz}}$	—	(−26)	—	dB
BPF frequency characteristics (4)	f_{BPF4}	f=3.58MHz. $\frac{\text{BPF lack}}{\text{BPF exists}}$	(−3)	(0)	(3)	dB
VCO free-run frequency	f_{CO}	No signal. Difference with f=3.579545MHz	(−300)	(0)	(300)	Hz
f_{CO} V_{CC} variation	$\Delta f_{CO/Vcc}$	Difference between V_{CC1}=9.9V/ and V_{CC1}=8.1V	(−300)	(0)	(300)	Hz
Demodulation output V_{CC} variation	$\Delta V_{C/Vcc}$	V_{CC1}=8.1V to 9.9V	(0)	(40)	(100)	mV_{P-P}/V
Static phase error	$\Delta\theta$	Tint deviation when fc=−300 to 300Hz change	—	—	(5)	deg/100Hz
Sub color control characteristics	ΔV_{subc}	Color level fluctuation portion when DATA 0A−5=1 V8=4V	(1.2)	(1.5)	(1.9)	times
RGB Processing Circuit						
C−Y/Y ratio	$R_{C/Y}$	Color bar input, measured at B out	(0.95)	(1.4)	(1.85)	times

■ Electrical Characteristics (cont.) (Ta=25±2℃)

Parameter	Symbol	Condition	min	typ	max	Unit
Differential gain	DG_Y		—	(3)	(5)	%
Pedestal level temperature variation	$\Delta V_{PL/T}$	Ta=−20 to +70℃	—	(−1.8)	—	mV/℃
Y_S switching speed	f_{YS}		(7)	(10)	—	MHz
External RGB input dynamic range	V_{DEXT}		(2.2)	(2.5)	(2.8)	V
Spot killer operation	V_{SPK}	V_{30}=9V, V_{12} voltage at which spot-killer operates	(7.8)	(8.1)	(8.4)	V
Internal/external crosstalk	CT_{RGB}	Leak in f=1MHz $0.2V_{P-P}$ Y_s=5V	—	(−60)	(−50)	dB
Synchronizing Signal Processing Circuit						
Horizontal output starting voltage	Vf_{HS}	f_O>10kHz when horizontal oscillation output is above $1V_{P-P}$	(4.0)	(4.5)	(5.0)	V
Lock detection output voltage	V_{LD}	In horizontal AFC lock	(5.7)	(6.0)	(6.3)	V
Lock detection charging and discharging current	I_{LD}		(±0.6)	(±0.8)	(±1.1)	mA
FBP slice level	V_{FBP}		(0.4)	(0.6)	(0.9)	V
Horizontal β curve	β_H		(1.3)	(1.7)	(2.1)	Hz/mV
Horizontal AFC μ	μ_H		(18)	(24)	(30)	$\mu A/\mu s$
Overvoltage protective operation voltage	V_{X-ray}	Tolerance of minimum voltage (V6V51/2) at which horizontal synchronization comes off	(−30)	(0)	(+30)	mV
Black-out operation voltage	V_{BLout}	Difference voltage from hold-down to black-out	(0.13)	(0.18)	(0.23)	V
IIC Interface						
Bus free before start	t_{BUF}		(4.0)	—	—	μs
Start condition set-up time	$t_{SU,STA}$		(4.0)	—	—	μs
Start condition hold time	$t_{HD,STA}$		(4.0)	—	—	μs
Low period SCL, SDA	t_{LOW}		(4.0)	—	—	μs
High period SCL	t_{HIGH}		(4.0)	—	—	μs
Rise time SCL, SDA	t_r		—	—	(1.0)	μs
Fall time SCL, SDA	t_f		—	—	(0.35)	μs
Data set-up time (write)	$t_{SU,DAT}$		(0.25)	—	—	μs
Data hold time (write)	$t_{HD,DAT}$		(0)	—	—	μs
Acknowledge set-up time	$t_{SU,ACK}$		—	—	(3.5)	μs
Acknowledge hold time	$t_{HD,ACK}$		(0)	—	—	μs
Stop condition set-up time	$t_{SU,STO}$		(4.0)	—	—	μs
DAC						
4bit DAC DNLE	L_4	1LSB=|DATA (0F) − DATA (00)|/15	(0.1)	(1.0)	(1.9)	LSB/STEP
7bit DAC DNLE	L_7	1LSB=|DATA (7F) − DATA (00)|/127	(0.1)	(1.0)	(1.9)	LSB/STEP
8bit DAC DNLE	L_8	1LSB=|DATA (FF) − DATA (00)|/255	(0.1)	(1.0)	(1.9)	LSB/STEP
7bit DAC DNLE (40)	L_{7-40}	3F→40	(0.1)	(1.0)	(2.9)	LSB/STEP
8bit DAC DNLE (80)	L_{8-80}	7F→80	(0.1)	(1.0)	(2.9)	LSB/STEP

Note) The characteristics value in parentheses is not a guaranteed value, but reference one on design.

■ Operational descriptions

• DAC CONTROL and SUB ADDRESS

SLAVE ADDRESS ; 8A

Control item	DATA BIT	Sub address	V_{CC}−ON	Remarks
COLOR	7	00	41	DATA 00→chroma off
TINT(HUE)	7	01	41	41=0100 0001
BRIGHTNESS	8	02	81	81=1000 0001
CONTRAST	7	03	41	———
SHARPNESS	7	04	41	———
CUT OFF(R)	7+1+(1)	05	81	0D−5 for (1)
CUT OFF(G)	7+1+(1)	06	81	0D−6 for (1)
CUT OFF(B)	7+1+(1)	07	81	0D−7 for (1)
DRIVE(R)	7+1	08	81	81=1000 0001
DRIVE(B)	7+1	09	81	———
Hor.CENTER	4	0A	09	09=0000 1001
VIDEO Adj.	4	0B	09	———
AUDIO Adj.	4	0C	09	———
BLUE BACK SW	1	0D−0	1	DATA 0→B BACK ON
AUDIO SW	1	0D−1	0	DATA 0→INT.
VIDEO SW	1	0D−2	0	DATA 0→INT.
BPF SW	1	0D−3	0	DATA 0→BPF ON
DELAY LINE SW	1	0D−4	0	DATA 0→D.L. ON
CUT OFF SW R	1	0D−5	0	DATA 0→OFF−SET OFF
CUT OFF SW G	1	0D−6	0	DATA 0→OFF−SET OFF
CUT OFF SW B	1	0D−7	0	DATA 0→OFF−SET OFF
Sub Color SW	1	0A−5	0	DATA 1→Black correction off, sub-color ON

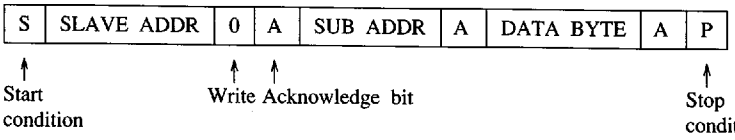
Note) (1) Values at power ON are not guaranteed, and initial setting should be required.
(2) For 7+1, the 7-bit DAC is changed over in two steps.
For 7+1+(1), the 7-bit DAC is changed over in four steps.

• I²C bus protocol

I²C−BUS Formats

(1) Slave address : 10001010

(2) Slave address format :



(3) Subaddress byte and data byte format :

Sub-addr' (H)	functions	Data byte							
		D7	D6	D5	D4	D3	D2	D1	D0
00	color	0	A06	A05	A04	A03	A02	A01	A00
01	tint	0	A16	A15	A14	A13	A12	A11	A10
02	brightness	A27	A26	A25	A24	A23	A22	A21	A20
03	contrast	0	A36	A35	A34	A33	A32	A31	A30
04	sharpness	0	A46	A45	A44	A43	A42	A41	A40
05	cutoff R	A57	A56	A55	A54	A53	A52	A51	A50
06	cutoff G	A67	A66	A65	A64	A63	A62	A61	A60
07	cutoff B	A77	A76	A75	A74	A73	A72	A71	A70
08	drive R	A87	A86	A85	A84	A83	A82	A81	A80
09	drive B	A97	A96	A95	A94	A93	A92	A91	A90
0A	H center	0	0	0	0	AA3	AA2	AA1	AA0
0B	Video Adj.	0	0	0	0	AB3	AB2	AB1	AB0
0C	Audio Adj.	0	0	0	0	AC3	AC2	AC1	AC0